



**Semiconductor
Technology Council**

**First Annual Report
September 1996**

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SECTION 1. EXECUTIVE SUMMARY

- ⚡ The Semiconductor Technology Council (STC) was established under the National Defense Authorization Act for Fiscal Year 1994 (Public Law 103-160) to advise the Secretary of Defense on matters relating to semiconductor manufacturing research and development (R&D).
- ⚡ The long-term health of the U.S. semiconductor and equipment industries is of paramount importance. The success of previous industry and Government R&D programs and coordination is evident. Industry has turned itself around, experiencing consistent revenue and market share growth over the past few years. Major challenges face this industry, however, and research funding must be increased, in coordination with more efficient development/commercialization activities, to meet future requirements and sustain growth in this critical industry.
- ⚡ National security is enhanced by a strong domestic semiconductor industry with leading-edge fabrication capabilities. The long-term health of the semiconductor industry depends on effective university research processes. Leading-edge capabilities are achieved through sustained levels of sufficient investment in strategic technologies and by effectively using all available R&D resources. University research efforts are important to the overall semiconductor R&D process, providing key strategic technology results and highly trained students with the specialized skills and expertise needed by industry.
- ⚡ Industry and Government are moving toward R&D funding models that are better suited to the present industrial position and capabilities. Industry is taking full responsibility for funding its mainstream infrastructure and is adapting its major cooperative R&D entities (SEMATECH and the Semiconductor Research Corporation [SRC]) to current needs and priorities. The Government is moving the emphasis of its major semiconductor fabrication R&D investments away from infrastructure toward longer range research. Programs at several departments and agencies (e.g., Department of Defense/Defense Advanced Research Projects Agency [DoD/DARPA], Department of Energy [DOE], and Department of Commerce/National Institute of Standards and Technology [DOC/NIST]) are moving toward efforts that will impact the 0.1 μm generation. As one example, with industry's endorsement, DARPA has created a new program to concentrate on strategic lithography technologies for 0.1 μm channel devices.
- ⚡ University fabrication facilities have not kept pace with industry capabilities because of the high capital and operating expenses needed to be at the leading edge. In response to these pressures, a few universities have formed flexible alliances and research networks to pool their distributed resources and expertise. Although these approaches are providing near-term mitigation, they do not solve the long-term issue of affordability. The capital and operating costs of maintaining leading-edge semiconductor fabrication facilities are increasing too rapidly for universities to afford those resources for the long term.
- ⚡ University approaches toward intellectual property rights and licensing practices have hindered the expansion of industry funding for research in some cases.



Key Recommendations

- ◆ Industry, Government, and academia should form a dynamic partnership, establishing a joint initiative to fund university research of strategic importance. An appropriate project funding, oversight, and operational framework should be implemented to accomplish the research goals and guide overall research efforts, protecting against the pressures of short-term business cycles and associated short-term needs.
- ◆ The partnership should pool its resources and increase the level of funding for long-term semiconductor research by sponsoring university efforts. The funding pool should be established by a pro rata increase over the next 3 years to a minimum, stable annual budget level of at least \$60 million, provided jointly by industry and Government on a 60 percent: 40 percent basis. This budget will increase university funding by more than 50 percent over current levels.
- ◆ Funding under this initiative is intended for long-term strategic research (impacts well beyond 5 years) to accelerate the expansion of technology options available to industry. A reasonable approach toward intellectual property and data rights should be applied up front and uniformly.
- ◆ Most research funding under this initiative should be applied toward technologies and approaches that will meet the requirements mapped out in The National Technology Roadmap for Semiconductors (NTRS or Roadmap). Research centers, distributed research networks, and proposals by individual investigators should be funded on a competitive basis to provide a diversity of researchers and a balance of technology approaches.
- ◆ Most of the partnership funding should be for efforts aligned with industry's Roadmap, but about 20 percent of the funding should be applied toward approaches not specified in the Roadmap. In either case, the funding and research direction should not be overspecified or linked too closely with manufacturing metrics, to protect against a shortened timeframe. Periodic project review will ensure progress, facilitate the exchange of ideas, and guide research.
- ◆ Creating lean management structures and processes that allow the new research initiative to retain a long-term strategic research focus will be key to the success of this endeavor.
- ◆ Universities will continue to have difficulty in maintaining leading-edge fabrication capabilities. Research networks may provide mitigation in some instances, but the long-term issues of high capital and operating costs remain. On the other hand, extremely useful, leading-edge research (and education) in this field can be accomplished at universities by moving toward sponsorship of physics-based investigations of process technologies, followed by scaling experiments to understand how those results transfer to and impact volume manufacturing practices. Experimental work is required to validate the theories of scaling, but these efforts are likely to be beyond the means of a single university. As appropriate, industrial facilities or national facilities, such as those at SEMATECH and the national laboratories, should be made available for university researchers to validate scaling models.
- ◆ Given the criticality of information technology in general and microelectronics in particular to the Department of Defense, DARPA should continue a robust program in advanced lithography research and develop a similarly sized program in microelectronics devices and manufacturing research for technologies off or beyond the Roadmap.

SECTION 2. INTRODUCTION

2.1 Background

The Semiconductor Technology Council (STC) was established by Congress under the National Defense Authorization Act for Fiscal Year 1994 (Public Law 103-160) to foster continued Government and industry cooperation in research and development for electronics and the semiconductor industry. The Council's charge is to build on past successes to help guide the public-private partnership in semiconductor R&D. The STC replaced a previous advisory body, the Advisory Council on Federal Participation in SEMATECH.

At the discretion of the cochair, one to four Council meetings are held annually. During its first year, the Council convened three times: November 21, 1994; March 28, 1995; and September 18, 1995. To fulfill its mission, the STC has created and chartered several task forces, as described in section 2.4.

Several dominant issues and themes concerning the status and direction of semiconductor research emerged at the first Council meetings. The major discussion topics were industry's funding trends, the roles and responsibilities of the stakeholders (i.e., industry, Government, universities, etc.) in sponsoring and performing semiconductor R&D, the status and direction of lithography R&D, the research environment at universities, and a developing proposal to create a new type of partnership for university research. This report focuses on the Council's examination of these issues.

2.2 Council Membership

The Council members are listed below:

Federal Government Members

Hon. Paul K. Kaminski, Cochairman
Under Secretary of Defense
(Acquisition and Technology)

Hon. Lionel (Skip) Johns
Associate Director for Technology
Office of Science and Technology Policy

Dr. Alexander MacLachlan
Deputy Under Secretary for R&D Management
U.S. Department of Energy

Hon. Laura Tyson
Assistant to the President for Economic Policy

Hon. Mary L. Good
Under Secretary for Technology
U.S. Department of Commerce

Dr. Neal Lane
Director
National Science Foundation

Presidential Appointees

Dr. Craig R. Barrett, Cochairman
Chief Operating Officer
Intel Corporation

Mr. Kenneth Levy
Chairman and CEO,
KLA Instruments Corporation

Mr. Steven R. Appleton
Chairman, CEO, and President
Micron Semiconductor, Inc.

Dr. John S. Mayo
President Emeritus
AT&T Bell Laboratories

Dr. Michael J. Attardo
General Manager
Microelectronics Division
IBM Corporation

Mr. Jack S. Kilby
J.S. Kilby Company

Mr. James W. Bagley
Vice Chairman
Applied Materials, Inc.
(now Chairman and COO,
OnTrak Systems, Inc.)

Dr. T.C. McGill
Fletcher Jones Professor of Applied Physics
California Institute of Technology

Mr. Hugh Barnes
Senior VP and General Manager
Portable PC Division
Compaq Computer Corporation

Mr. George Sollman
President and CEO
Centigram Communications Corp.

Executive Director

Dr. Lance A. Glasser
Director, Electronics Technology Office
Defense Advanced Research Projects Agency
(now VP of Advanced Programs, KLA
Instruments Corp.)

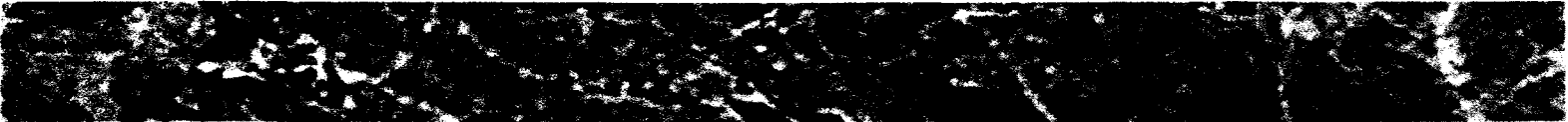
2.3 Council Objectives and Functions

According to the establishing legislation, the objectives of the Council are as follows:

- ◆ Link assessment by the semiconductor industry of future market and national security needs to opportunities for technology development through cooperative public and private investment;
- ◆ Seek ways to respond to the technology challenges for semiconductors by fostering precompetitive cooperation among industry, the Federal Government, and institutions of higher education;
- ◆ Make available judgments, assessments, insights, and recommendations that relate to the opportunities for new R&D efforts and the potential to better rationalize and align industry and government contributions to semiconductor research and development.

According to the establishing legislation, the Council shall perform the following functions:

- ◆ Advise SEMATECH and the Secretary of Defense on appropriate technology goals and appropriate level of effort for the research and development activities of SEMATECH.
- ◆ Review the emerging markets, technology developments, and core technology challenges for semiconductor R&D and semiconductor manufacturing and explore opportunities for improved coordination among industry, the Federal Government, and institutions of higher education regarding such developments and challenges.
- ◆ Assess the effect on the appropriate role of SEMATECH of public and private sector international agreements in semiconductor research and development.
- ◆ Exchange views regarding the competitiveness of U.S. semiconductor technology and new or emerging technologies that could affect national economic and security interests.
- ◆ Exchange and update information and identify overlaps and gaps regarding the efforts of industry, the Federal Government, and institutions of higher education in semiconductor research and development.

- 
- ◄ Assess technology progress relative to industry requirements and Federal Government requirements, responding as appropriate to the challenges in the national semiconductor technology roadmap developed by representatives of industry, the Federal Government, and institutions of higher education.
 - ◄ Make recommendations regarding the semiconductor technology development efforts that should be supported by Federal agencies and industry.
 - ◄ Appoint subgroups as appropriate in connection with the updating of the semiconductor technology roadmap.
 - ◄ Publish an annual report addressing the semiconductor technology challenges and developments for industry, government, and institutions of higher education and the relationship among the challenges and developments for each, including an evaluation of the role of SEMATECH.

2.4 Task Forces

To support its objectives and to perform its functions, the Council created the following four task forces to focus on specific issues:

- ◄ *Research and Development Funding Task Force*
 - Mission: Develop an understanding of public and private funding of semiconductor R&D to illuminate the investment strategies of major international stakeholders
 - Members: C. Barrett (leader), S. Appleton, L. Johns, K. Levy
- ◄ *University Research Funding Task Force*
 - Mission: Clearly assess the adequacy of funding and infrastructure at universities and provide insight on the future roles of universities in the semiconductor industry
 - Members: J. Bagley (leader), C. Barrett, J. Mayo, T. McGill
- ◄ *Decision-Making Process Task Force*
 - Mission: Examine existing processes for Government-private sector interaction and recommend processes or modifications that would lead to better synchronization
 - Members: P. Kaminski (leader), C. Curtis, L. Johns
- ◄ *Focus Area Task Force*
 - Mission: Building on The National Technology Roadmap for Semiconductors, identify critical technology gaps and roadblocks, then estimate the cost to overcome those obstacles to progress
 - Members: M. Attardo (leader), J. Bagley, J. Mayo, T. McGill

At the September 18, 1995, meeting, as an adjunct to the Focus Area Task Force, a special task force on lithography also was chartered by the Council to provide input and recommendations on an R&D strategy for lithography. This task force received staff support from SEMATECH.

SECTION 3. STATUS OF SEMICONDUCTOR R&D

Semiconductor integrated circuits (ICs), interchangeably referred to as semiconductors within the context of this annual report, are produced by a complex sequence of some 500 to 700 unit manufacturing processes performed on a fabrication line in a factory. Unit processes include the deposition and etch of thin films, pattern transfer from the mask to the wafer, wafer surface preparation, implantation of dopant species, and thermal cycles. New factories may cost as much as \$1 billion or more, exclusive of process development expenses. Typically, a fabrication line is dedicated to manufacturing a single technology generation. A semiconductor technology generation, often referred to by its minimum line width (e.g., 0.25 μm , 0.18 μm), essentially requires its own toolset and manufacturing processes and is generally replaced every 3 years by the next generation. In other words, an IC technology generation has a 3-year lifetime at the leading edge of semiconductor technology. Of course, older technology generations may be used for much longer than 3 years for IC production.

3.1 Brief Overview of Recent and Expected Future Industry Health

The purpose of this report is to provide a brief overview of semiconductor industry performance, not to analyze market details or to forecast future performance. Numerous publications and market research services are available that analyze the indicators of the health of and likely future for the semiconductor industry, both economic- and technology-based (Dataquest, Rose and Associates, VLSI Research, and Integrated Circuit Engineering Corporation [ICE] produce various types of reports and analyses, for example).¹ The intent here is to highlight industry's recent general performance, especially as it pertains to the funding of advanced research. Most of the data and analysis of the semiconductor IC and applications markets presented in this report were derived from ICE Status 1996² and presentations to the Council. By most accounts and standards, the semiconductor industry has done well recently from a revenue standpoint. However, a number of factors other than revenue may influence the investments in semiconductor R&D by both industry and Government.

3.1.1 Recent Performance and Observations

In 1995, the global merchant semiconductor industry had revenues of about \$148 billion, with about \$128 billion in the integrated circuit sector and \$20 billion in discrete components.² It is estimated that the equivalent value of captive production worldwide was about \$6 billion in 1995. In 1994, the revenue of merchant semiconductor IC producers was about \$90 billion. The revenue growth of merchant semiconductor companies in 1995 was therefore about 42 percent over 1994. Revenue growth in both 1994 and 1993 exceeded 30 percent. Since 1990, the cumulative annual growth rate for the merchant IC industry has been 21 percent. Figure 3-1 shows 5-year averaged growth rates, along with world market size. Worldwide unit volume shipments increased by almost 18 percent in 1995, so much of the revenue growth was the result of an increased average selling price of products.

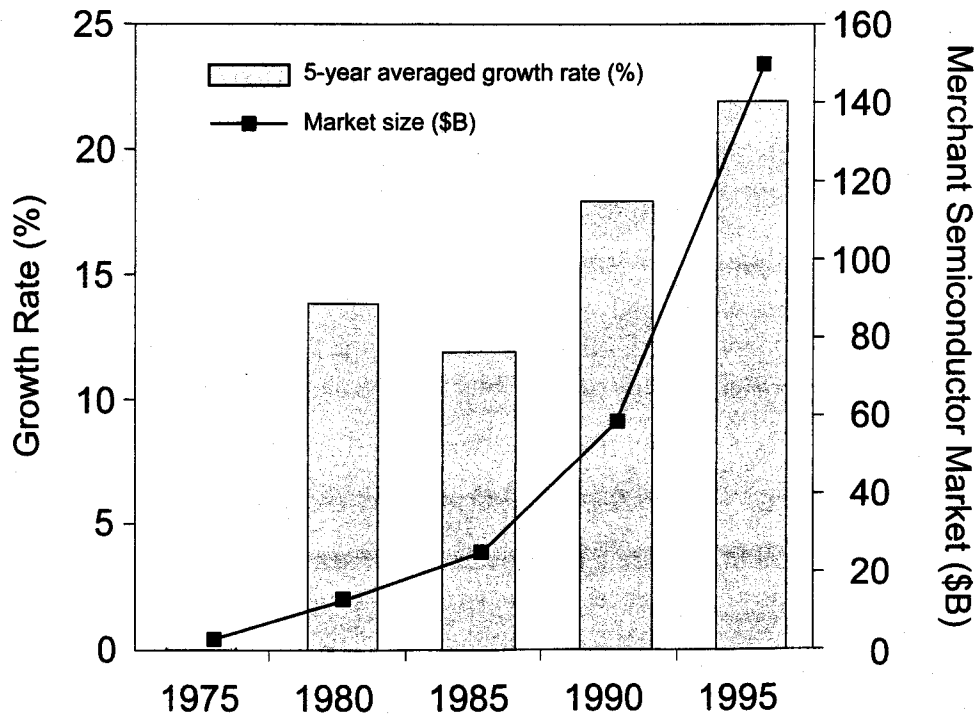


Figure 3-1. Semiconductor Industry Growth Trends

In 1995, U.S. companies captured about 42 percent of the world market for semiconductors, while Japanese companies held about 36 percent, Korean companies about 10 percent, European companies about 7 percent, and the rest of the world, mainly other Pacific Rim nations, about 5 percent. This is the third year that U.S. and Korean merchant semiconductor companies have increased their market share, while that held by Japanese and European companies has declined.

The U.S. end-use market is driven mainly by data processing applications (73 percent) and communications (14 percent). The Japanese market has a sizable consumer electronics sector (23 percent), as well as data processing (51 percent) and communications (12 percent) sectors. Personal computers (PCs) are the dominant component of the data processing market, and a PC has a relatively high semiconductor content by value (35 percent of total is typical). Sustained, strong growth in PC demand in 1995 was a major factor driving the growth in the semiconductor industry that year. In general, the relative value of the electronic content of systems is increasing (see figure 3-2). An increasing worldwide demand for new telecommunications products from both industrialized and emerging countries appears to be a strong driver for semiconductors over the next decade. It is also interesting to note that, in 1994, consumer electronics represented about 32 percent of the Japanese end-use market. The Japanese recession and a lack of new products contributed to the 1995 decline.

Although industrial revenues have grown, to be at the leading edge in semiconductor manufacturing has become increasingly expensive. Great financial risks are involved in matching production capacity with demand, because of the high cost to purchase and operate semiconductor manufacturing equipment and maintain production capacity.

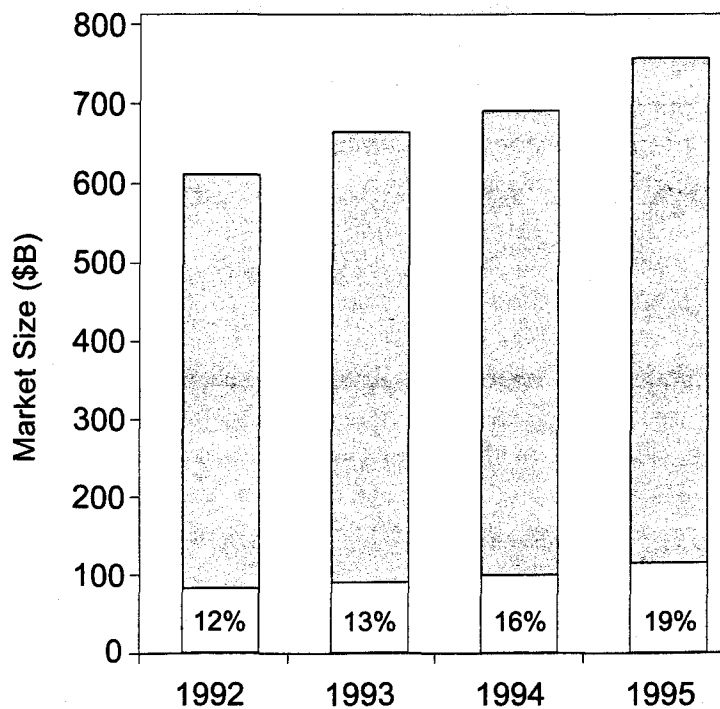
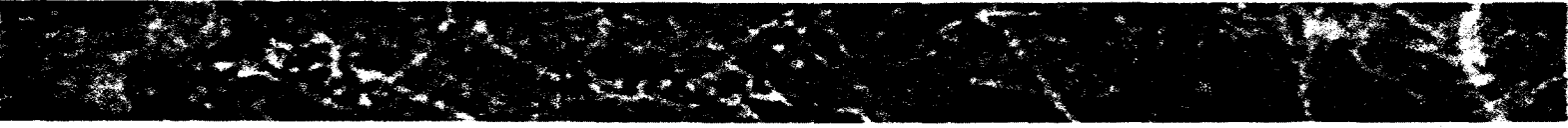


Figure 3-2. Electronic System World Market, Indicating the Proportional Value of the Electronics¹

Since 1992, the global semiconductor industry's capital expenditures have averaged just over 20 percent of sales, a level that is viewed as sufficient to meet the projected capacity demands cost-effectively.² Numerous companies have spent far more on average, though, adding production capacity at record rates. In the United States, expenditures by Intel, Motorola, Texas Instruments, and IBM alone account for well over half of the entire U.S. industry investment. Ever-increasing chip complexities, larger chip active areas, more interconnect layers, and additional process steps are continuing to increase manufacturing costs. New factories may well cost more than \$1 billion, depending on factors such as location, size, capacity, and expandability. Throughout the semiconductor industry's history, manufacturing productivity enhancements have allowed the industry to keep pace with the cost of manufacturing reinvestment. Productivity is discussed in more detail below.

The health of the semiconductor materials and equipment (SME) industry directly depends on the health of the semiconductor industry. In 1995, the global SME industry had revenues of about \$47 billion, with \$31 billion in the equipment sector (including test and assembly) and \$16 billion in materials and consumables (e.g., wafers, gases, masks, chemicals). The semiconductor equipment supplier industry is dominated by U.S. and Japanese companies, although some notable European companies have well-established markets. The revenue growth of equipment companies in general during 1995 was rather substantial in that the total 1994 revenues were just over \$13 billion for equipment.³ In general, semiconductor manufacturing equipment has increased in production capability, throughput, and cost, yet has not increased in useful lifetime. About 70 percent of the cost of a new factory is for equipment.⁴



Many tool suppliers are now at the limits of their production capabilities. With the possible exception of those companies producing lithography exposure tools, an average U.S.-based supplier of semiconductor process tools has expanded and increased revenue over the past several years. Although these trends may continue as long as the semiconductor industry grows, intense competitive pressures have forced suppliers to decrease their research investments in future technologies. This is a concern, because the effective tool lifetime for leading-edge production often is only a single technology generation. It typically takes a long time to fully develop, commercialize, and field a new piece of process equipment based on a new technology or approach. Also, developing new tools is becoming extremely expensive as process requirements for future technology generations become more stringent. Although supplier revenues have increased, small discretionary R&D budgets and high R&D costs may make it difficult to recover from the present reduced rate of corporate research expenditures to accelerate the availability of new tools and processes for future technology generations. Whether or not this situation constitutes a risk to the health and security of the domestic semiconductor industry is under debate, although it is clearly prudent for the industry to not depend on a single overseas supplier for any critical technology.

Although past performance, forecasts, and market studies are not always conclusive evidence of an industry's long-term future health, when coupled with other trends, such as capacity utilization rates, these indicators usually are reliable. Utilization rates are presently greater than 50 percent, and, historically, the industry has been able to show profits when this is so. The growth rate of the industry may slow in the future, but growth is expected to continue in the end-use markets for computers and communications; thus, if the domestic semiconductor industry can position itself, the potential exists for continued expansion. By some estimates, the world merchant semiconductor IC industry will more than double by the year 2000. The equipment and materials supply industries can therefore reasonably expect the growth of the semiconductor producers to spill over and directly affect their business sectors as well.

Thus, there appears to be an excellent environment for domestic semiconductor companies and their supplier tiers to continue expanding or maintaining world market share. There are no guarantees, however; the global semiconductor business is extremely competitive and aggressive attempts by new regions to capture market share will create additional pressures. To remain a viable global competitor, the domestic semiconductor industry must be able to fund its own expansion and research, in coordination with federally sponsored research, in the areas with overlapping interests.

3.1.2 Productivity

Productivity is a primary focus in the manufacture of semiconductor integrated circuits, from that of individual equipment to that of work cells, factories, manufacturing practices, circuit designs, and methodologies. Two common metrics used to gauge productivity—the value added per employee and the profit per employee—have risen about 13 percent annually since the mid-1980s among U.S. manufacturers, an indication of the domestic industry's productivity. Figure 3-3 shows another measure of productivity, the declining cost per bit of dynamic random access memories (DRAMs). Analogous data could be plotted for other segments, such as metal oxide semiconductor (MOS) logic, and would reveal a similar annual decline in cost per function. The semiconductor industry

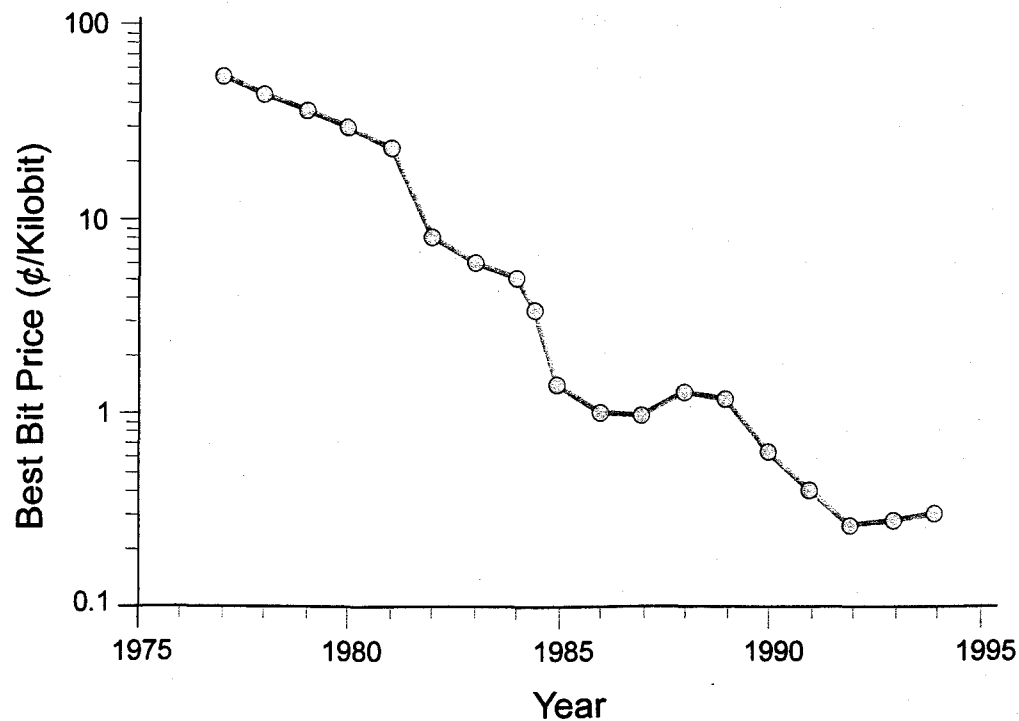


Figure 3-3. Measure of Manufacturing Productivity—Declining Cost per Bit of Dynamic Random Access Memories, a Commodity Component

has maintained yearly component cost reductions (and component improvements) of about 30 percent. In the past, productivity has been enhanced through product design innovations, linewidth reduction, increased chip areas and wafer sizes, yield enhancements, parallel processing, and increases in overall equipment efficiency. Product yields are now sufficiently high that productivity cannot be improved further by this means.

Numerous approaches, however, remain to be fully exploited for continued productivity enhancement. Besides company-instituted design/process innovations, continuing improvements in the industry's productivity will now involve closer industry coordination and standardization, such as those required to cost-effectively and efficiently progress toward the use of 300 mm diameter silicon wafers (current de facto industry standard is 200 mm). The use of larger diameter wafers is very attractive from a productivity standpoint, because the operating and consumables costs are approximately 40 percent higher than for a 200 mm tool, yet the potential number of chips is much greater, more than double. A change in wafer diameter, however, will require a new set of manufacturing tools and wafer handlers, although, in principle, no insurmountable technical obstacles are apparent in developing tools and processes for 300 mm silicon wafers. Additional aspects and issues regarding the conversion to 300 mm wafers and tools are discussed in more detail in section 4.2.

3.2 Structure and Nature of Public/Private R&D Funds

3.2.1 Research Investment Profile

Since 1980, the annual growth rate of industry-sponsored semiconductor research has averaged about 16 percent. In the current year, industry will spend about \$6 billion on R&D. In terms of annual revenues over the past year, the U.S. semiconductor industry invested about 12 percent in R&D, while Japan invested about 14 percent, Europe about 12 percent, Korea about 17 percent, and Taiwan about 5 percent. Research investment calculated as a percentage of revenues has decreased by about 2 percent annually over the past 2 to 3 years, except in Korea, where the investment has increased from 4 percent of revenues (in 1992) to 17 percent today. The research investments of regional industries and their governments from 1990 to 1994 are shown in figure 3-4. The annual private research investments of the semiconductor industry as a function of geographic location are shown as a percentage of total revenue in figure 3-5. These figures show that the total spent by U.S. semiconductor companies on R&D is increasing in absolute terms, but not as a percentage of revenue.

The investment in R&D by U.S. and Japanese equipment suppliers is about 13 percent and 7 percent of their respective revenues, although additional Japanese R&D investment likely falls under the "sales" classification and is not reflected here. Equipment companies have experienced

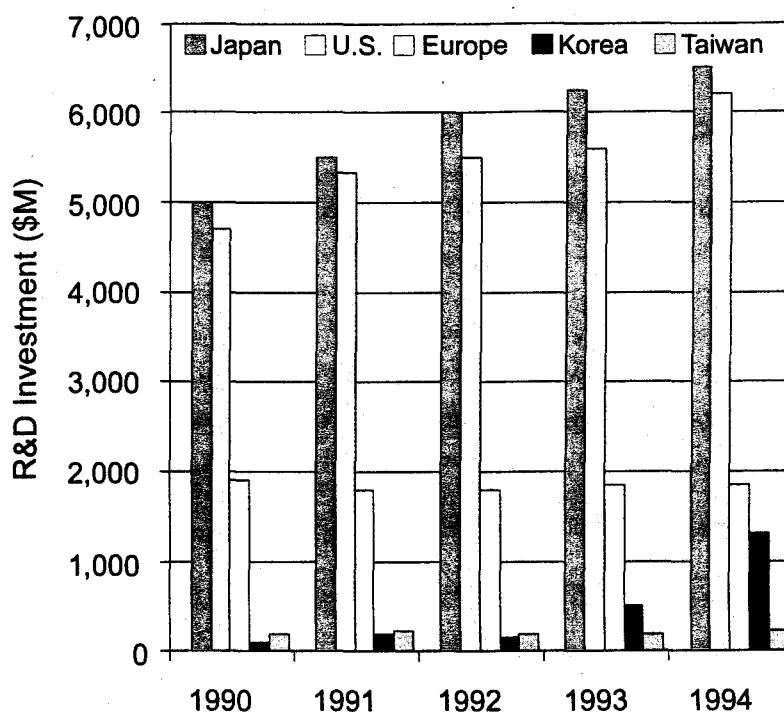


Figure 3-4. Research Investments by Regional Industries and National Governments from 1990 to 1994

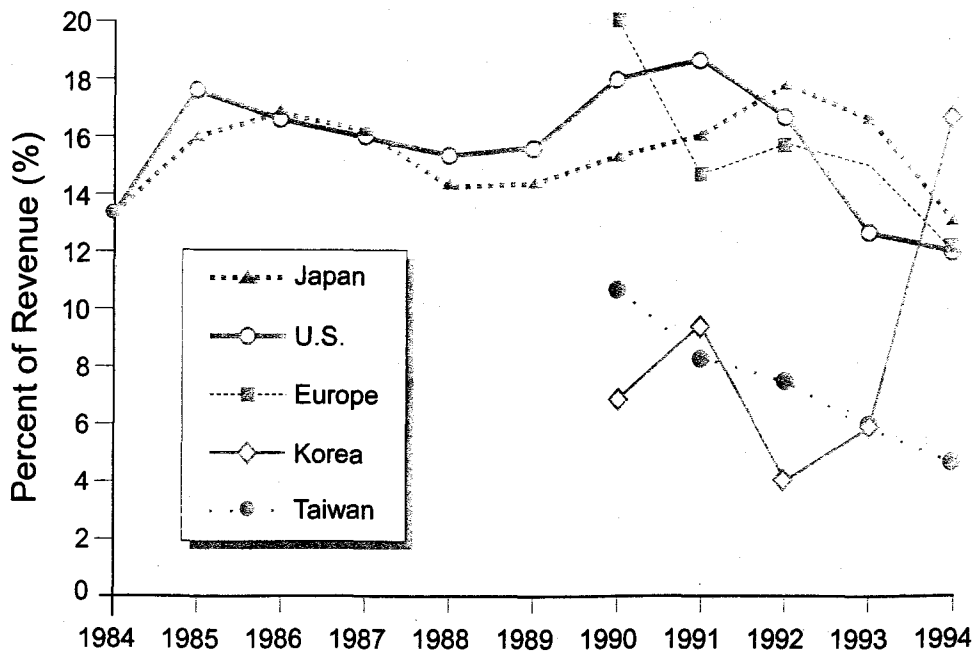


Figure 3-5. Annual Private Research Investments of the Semiconductor Industry as a Function of Geographic Location, Shown as a Percentage of Total Revenue

revenue growth over the past few years in conjunction with the semiconductor industry, so the total dollar amounts for research are increasing, but not as a percentage of company revenues. Both U.S. and Japanese equipment companies have decreased their percentage of revenue on research since a recent peak in 1992. Most funded efforts are for near-term equipment improvement and incremental model evolution, not for long-range research of new tool concepts. Growth of the semiconductor industry may not be sustained unless supplier research resources can be increased.

Public and private investment in U.S. semiconductor R&D shown in figure 3-6. Although the exact figure somewhat depends on how individual efforts are classified, in fiscal year 1995, the U.S. Government invested about \$600 million of public funds in research for areas of interest to the semiconductor industry, or about 10 percent of the total R&D by dollar value. Approximately half of the total funding from the Government (\$300 million in FY 96) is for technologies directly applicable to merchant IC manufacturers. The rest of the funding may be of niche or indirect importance. It is evident from figure 3-6 that, over the past few years, the U.S. Government consistently has funded 10 percent of the total sponsored research. Considerable additional research is sponsored by the U.S. Government in specialized technology areas that usually are not directly applicable to the industry in general, such as those specifically for defense purposes. Radiation hardening of electronics for survival through irradiation by a nuclear event is one example. Further microelectronics-related R&D is sponsored by Government agencies in support of specific systems or platforms, such as those for future DoD missile and avionics systems.

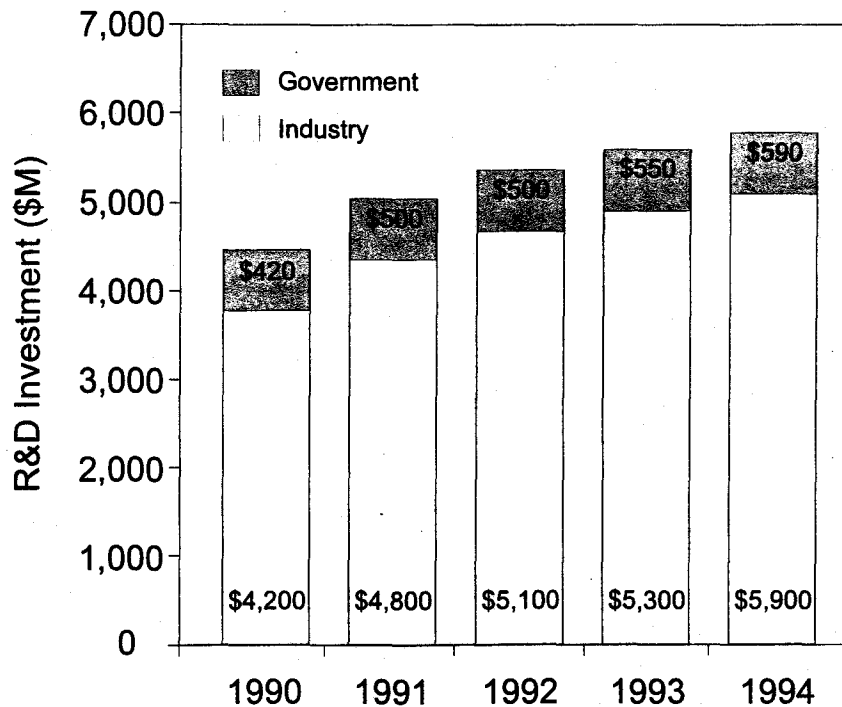


Figure 3-6. Public and Private Investment in Semiconductor R&D in the United States

At present, the annual DoD budget is forecast to decline, including funds allocated for research, development, test, and evaluation (RDT&E). As DoD budgets decline, the relative amount of funding available for sponsored semiconductor research is likely to decline as well. This decline may not have an adverse effect on the semiconductor industry, because the industry has sufficient revenue to fund and perform the R&D necessary to sustain its present growth rate. Near-term issues, including present and next-generation technologies, are the domain of industry. It is apparent that the difficulties in developing technologies and approaches for manufacturing semiconductors beyond the next generation will require an effort greater than that required to produce the preceding generation. It is also clear that a coordinated, strategic response by industry toward the funding of its R&D will help sustain long-term growth, despite less Federal R&D funding. Industry must assume the primary responsibility for near-term development and infrastructure issues. The focus of Federal R&D funds should be shifted from near-term R&D, or infrastructure building, to much longer term research issues, such as an accelerated effort in the equipment, processes, and approaches to fabricate classes of ICs beyond the traditional MOS paradigm. Industry also should be more proactive in sponsoring research efforts for technologies beyond the next generation. In areas of common interest, joint R&D funding is attractive to increase leverage and reduce risk.

Governments worldwide are interested in developing or preserving a national or local semiconductor industry (see figure 3-4). Cooperation with industry may take on various forms, from contracts and grants, to tax relief, to other economic assistance. Foreign governments also have entered into R&D partnerships with industrial firms to advance the local semiconductor industry with different operational approaches and variable success. Major efforts are shown in figure 3-7.

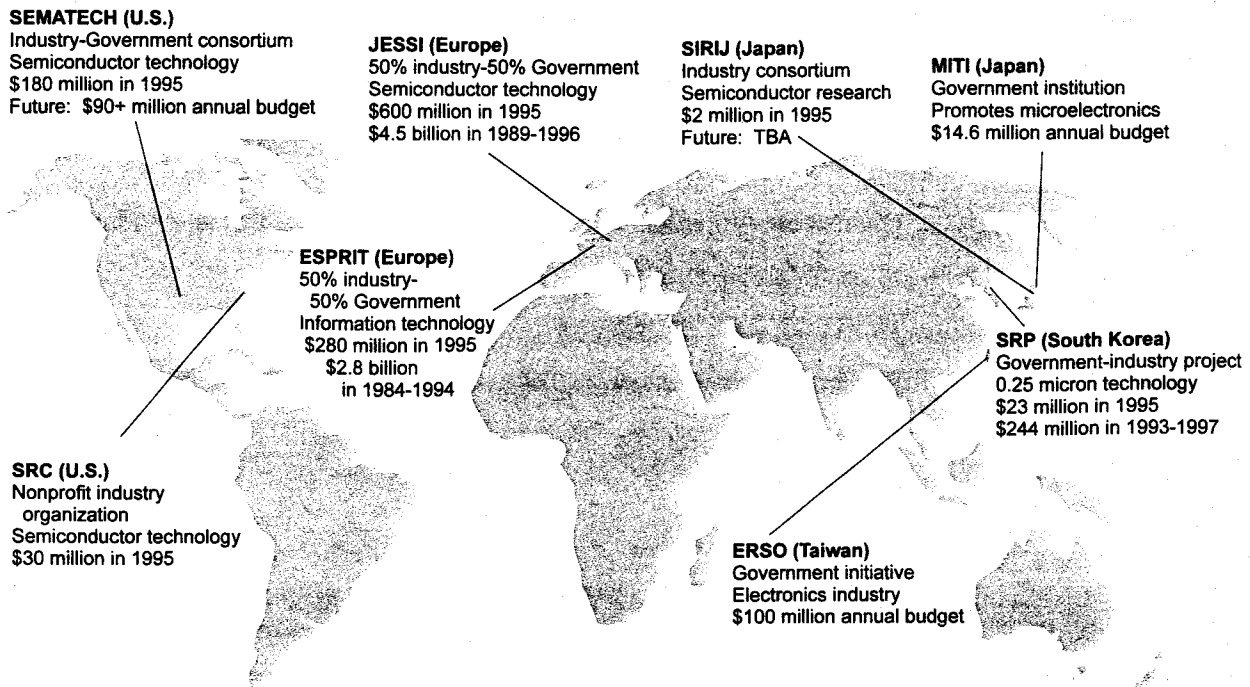
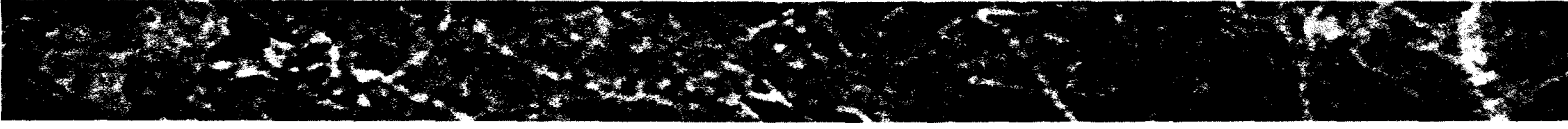


Figure 3-7. Summary of Major Industry-Government Cooperative Semiconductor R&D Organizations

National trade, taxation, and regulatory policies and political environments dramatically affect any industry. This report is not intended to comprehensively present any regional or national comparisons. Rather, the intent is to provide some insight into how various governments treat semiconductor R&D. In the United States, State and local governments may provide special economic or tax benefits to IC companies opening major semiconductor facilities. In an indirect sense, the savings then may be applied toward increased R&D or capital outlays in facilities. In addition, the U.S. Government (and industry) sponsors R&D efforts through contracts, grants, or other agreements with industrial firms, universities, or Government-owned laboratories in areas that relate to the specific mission of the sponsoring agency. As an example of a major initiative, the Department of Defense has provided funding to SEMATECH since its inception in 1987. Involvement by the Japanese Government is similar. The Japanese Government has funded a larger percentage of research, 17 percent versus 10 percent in the United States by dollar value. Japan has the highest total expenditures on R&D, although Korea has the largest increase in R&D investment. The Japanese Ministry of International Trade and Industry (MITI) has planned a 5-year project, funded at \$100 million the first year, to focus on next-century technologies. The project is being performed by a consortium of 10 of Japan's largest electronics firms, numerous equipment and materials companies, and several foreign capital companies. The Korean Government does not directly invest much in industry R&D efforts, but special tax and other incentive credits are commonly awarded to firms—in effect, lessening capital burdens and freeing revenue. The Korean legislature has adopted favorable tax laws to encourage the repatriation of foreign-trained engineers. Korean corporate taxation is relatively favorable compared with that in the rest of the world. Government-owned



science parks provide low-cost facilities for R&D, and the government also provides low-interest-rate loans for certain purposes. Taiwan appears to be following a strategy following closely behind the technology leaders, as indicated by its low rate of research investment, but continued revenue and capacity growth. The Taiwanese Government also provides research facilities for industry and assists in spinning off companies from sponsored R&D initiatives. Low corporate income taxes for semiconductor manufacturers also are typical in Taiwan. Total spending by European industry and government on semiconductor-related R&D appears to be flat, exhibiting the highest percentage of government participation.

3.2.2 Classification of Time Horizon

The cyclical nature of IC technology introduces a new generation of processes and associated devices and circuits about every 3 years, preceded by considerable R&D on the tools, unit processes, process integration, and general manufacturing procedures. At any given time, essentially three different process generations are in various stages of completion. The present generation, denoted as G , is undergoing incremental improvements and maintenance. The next-generation, $G+1$, is under final development and integration, while $G+2$ is still in R&D. Figure 3-8 is a profile of an R&D time horizon classification by a typical company. As shown, just under 60 percent of the effort, by dollar value, is in near-term development, solving product-specific development issues, while just under 40 percent focuses on next-generation development, a sum total of over 95 percent of the total internal funding available. The remaining budget, 4 percent, is invested in research for $G+2$ or beyond. Also of interest is the breakdown of efforts for one particular company, shown in figure 3-9. Most investment clearly is in solving specific product and process development issues. The breakdown will vary among companies, but, in essentially every case, most investment is expected to be in product development, not long-term research.

Assuming that most companies do not differ dramatically, it can be expected that, of the \$5.9 billion investment by semiconductor companies in 1995, \$3.4 billion was for G , \$2.4 billion was for $G+1$, and \$0.3 billion was for issues beyond $G+2$. Corporate investment in the Semiconductor Research Corporation (SRC) totaled about \$30 million in 1995 and therefore represents about 10 percent of the industrial efforts for $G+2$. SRC typically sponsors university research focused on long-term research issues (i.e., those beyond $G+1$). A typical industry attitude is to not expend time and internal resources in solving long-term issues through somewhat risky research, when many nearer term issues require attention.

The time horizon of the equipment manufacturers' R&D is skewed toward that of the semiconductor industry. Historically, a typical R&D profile for an equipment supplier is about 70 percent emphasis on G , 25 percent on $G+1$, and 5 percent for issues beyond $G+2$. In contrast, the major emphasis from Government funding agencies is on $G+1$, $G+2$, and beyond. The present generation receives relatively little attention, because it is the domain of the mainstream industry. DARPA is funding major electronics R&D initiatives, including micro-electromechanical systems (MEMS), optical technologies, advanced packaging technologies, device technologies beyond MOS, and semiconductor technologies for various applications (e.g., high temperature, data conversion,

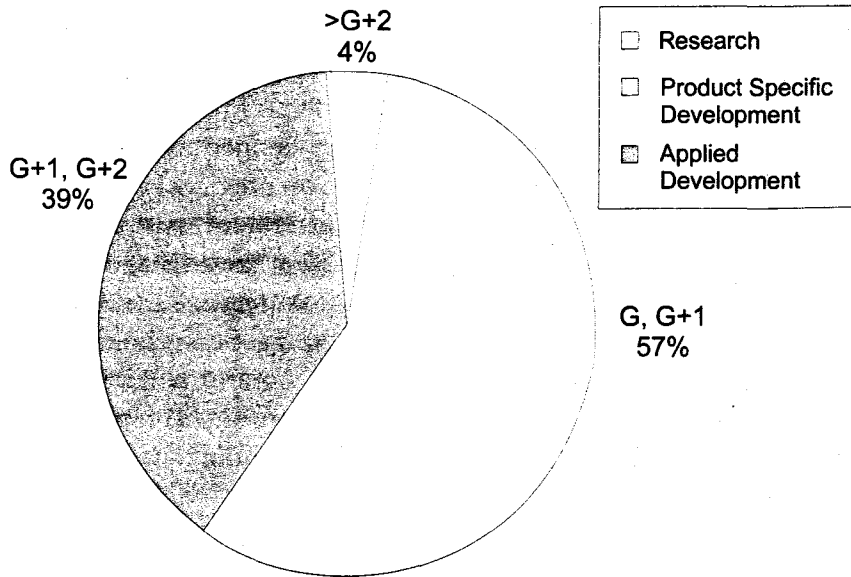


Figure 3-8. Profile of R&D Time Horizon Classification for a Typical Merchant Company

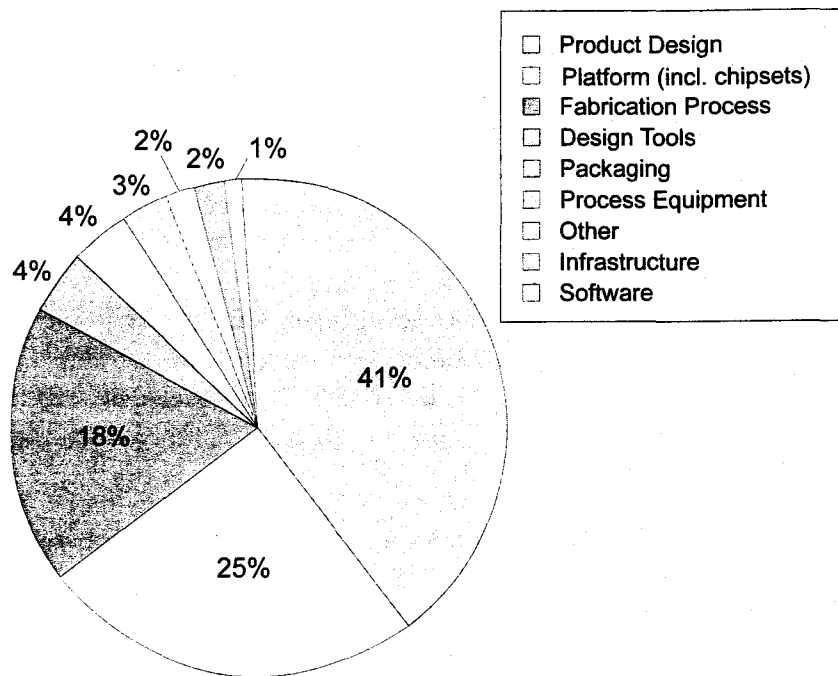
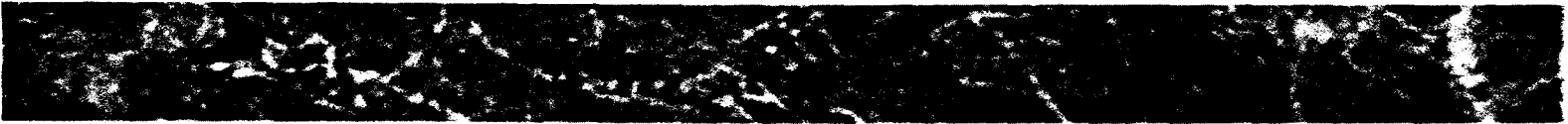


Figure 3-9. Breakdown of Privately Funded R&D for a Typical Merchant Semiconductor Company




low-power dissipation). DARPA also has funded the SEMATECH program and various efforts under the National Center for Advanced Information Component Manufacturing (NCAICM), efforts of direct, near-term interest to the mainstream semiconductor and equipment industries.

Classification of the time horizon is a perception issue. Federal Government R&D managers consider industry's research programs to be incremental and very applied, while industry managers view these same programs as too risky to pursue alone. As shown previously, the annual revenues of the semiconductor and equipment industries are anticipated to continue growing. Merchant semiconductor industry revenues already exceed \$100 billion annually and are projected to increase to more than \$1 trillion in the next 10 to 15 years. In Washington, the trend is toward downsizing the Federal Government and reducing the growth rate of the Federal budget. It is unrealistic to assume that the growth in federally supported electronics research will keep up with the projected growth of the industry itself. Thus, it is imperative for the industry to continue with the trend it has demonstrated with SEMATECH, taking responsibility for funding and performing the near-term development and infrastructure support necessary for long-term viability as an industry. It also is critical for industry to take a greater role in funding suppliers or external entities to develop technologies with major applications beyond *G+1*. Given its relative strength, the industry also should increase its internal funding of technologies for applications beyond *G+1*. Increasing funds for leveraged entities such as SRC or SEMATECH is a way to fulfill these responsibilities through shared risks and rewards. A method for linking *G+1* researchers with users is necessary. This linkage must be strong enough to ensure proper focus and interest, yet not so strong that creativity is stifled. Federal R&D support should focus on strategic technology advancement, accelerating progress in new approaches or in narrowing options for the *G+2* generation, with minimal effort on near-term technologies aligned to The National Technology Roadmap for Semiconductors.

3.2.3 Major U.S. Industry-Funded R&D Entities and Efforts

The Semiconductor Research Corporation is an organization with about 60 member companies that sponsors and manages research at U.S. universities. The SRC is presently sponsoring research activities at about 50 academic institutions, including several multidisciplinary research centers. The SRC is credited with being a major source of research funding for university efforts in mainstream IC technology areas, such as silicon complementary metal oxide semiconductor (CMOS) manufacturing. The corporation wants to meet research needs that are directly aligned to industry needs and to provide well-trained graduate students. Historically, the SRC has been most productive on task-level projects. Even multidisciplinary centers are involved with several tasks rather than an integrated effort. SRC projects are best suited for application beyond *G+1*, with some exceptions in computer-aided design (CAD) areas, where impacts to *G* and *G+1* are expected.

In recent years, member companies have been providing the SRC with an annual budget of \$35 million. Before 1996, the SRC's budget was capped at a fraction of its members' revenues and had not increased in the previous few years, despite member company revenues increasing from 10 percent to 75 percent annually (21 percent average annual growth in aggregate merchant IC revenues since 1990).² Before FY 96, SEMATECH had been funding the SRC with about \$10 million annually (\$5 million from the DARPA grant and \$5 million from industry) to manage SEMATECH's



university centers of excellence program. In FY 96, SEMATECH provided about \$8 million to the SRC. Beyond FY 97, SEMATECH is not planning to continue SRC funding, although SEMATECH plans to strengthen its ties and technical interactions with the corporation. In response to this decrease in funding, SRC members have altered the formula by which dues are calculated to make up the budget difference. The dues revenue cap was increased, and provisions were adopted for annual budget growth from inflation and a rising research "cost of living."

SEMATECH, a semiconductor manufacturing research consortium based in Austin, Texas, consists of 10 corporate member companies and DoD, as represented by DARPA. From 1988 to 1996, SEMATECH members had been contributing \$90–100 million annually with 1:1 matching funds from DARPA. SEMATECH's stated mission is to solve the technology challenges required to keep the United States number one in the global semiconductor industry. Member companies have placed employees in temporary rotating assignments at SEMATECH, and direct hires are employed as well. SEMATECH is organized into thrust areas that are aligned with the Semiconductor Industry Association's (SIA) National Technology Roadmap for Semiconductors. Thrust areas sponsor and manage external R&D efforts with semiconductor manufacturers, equipment suppliers, and universities, and also execute internal programs. About 60 percent of SEMATECH's annual budget is now expended on external R&D efforts. In most cases, those efforts are highly leveraged with additional funds from industry or in-kind contributions of time and facilities. SEMATECH has worked very hard to maximize technology transfer to member companies. Overall management and guidance of the consortium comes from the Board of Directors and a hierarchy of technical advisory boards with member company representation.

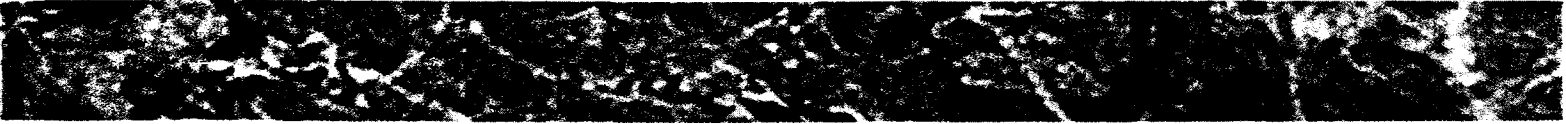
In July 1994, the SEMATECH Board of Directors adopted a resolution, thanking the Federal Government for its partnership with the semiconductor industry in SEMATECH, which spurred industry's turnaround, and helped in regaining world competitiveness. With the anticipation of the domestic industry's continued good health, the SEMATECH Board of Directors voted to transfer all of SEMATECH's operation to private funding beginning in 1997. Although the board stated that continued Government R&D investment was critical, they believe that those funds should flow directly to researchers rather than through SEMATECH. In FY 96, about \$89 million of public funds were appropriated for SEMATECH by Congress. For the years following this final increment of DARPA matching funds, SEMATECH is planning for steady annual funding of about \$120 million beginning in 1997. SEMATECH is now determining its specific long-term technology and strategic operating plans. Under the reduced annual operating budget, SEMATECH's mission may change to provide critical-mass efforts to solve challenges in selected critical technology focus areas. For example, major efforts in the development of lithography tools are anticipated, specifically in final development and commercialization of 193 nm wavelength technology. Infrastructure development and technology coordination roles are expected to continue in the wafer fabrication sciences. SEMATECH also has been expanding its mission to upstream and downstream technology areas, such as design, test, assembly, and packaging. The long-term levels and types of activities within thrust areas are still being determined.

3.3 Roadmap-identified Technology Needs and Barriers

The SIA and SEMATECH have jointly sponsored efforts leading to the production of a document describing the future technology needs of the semiconductor industry. That document, The National Technology Roadmap for Semiconductors (referred to as NTRS or the Roadmap), is the product of efforts by several working groups with participants from industry, academia, Government, and other areas under the guidance of the Roadmap Coordinating Group.⁴ Two editions of the NTRS have been released, the first in 1992, then a completely new update at the end of 1994. The Roadmap is a requirements document and lays out many, but not all, of the technology options that may meet the projected manufacturing requirements. Full implementation of the Roadmap will be much more costly than it is today or as planned for the next few budget cycles.

The opinion of the community that produced the Roadmap is that a gap exists in funding for several critical technology areas. Estimates are that industry is now funding about \$180 million in research, including funding of the SRC, that applies directly to the Roadmap, while the Government is providing about \$150 million for relevant research. In total, the research gap—those areas not funded but required to meet the needs identified in the Roadmap—is estimated to be about \$450 million in 1996. Despite the trend toward short-term, product-driven R&D by industry, the Focus Area Task Force identified five particular technology areas that are underfunded to meet the demands predicted by the Roadmap. Whether or not this gap is a threat to the domestic semiconductor industry or its productivity enhancement is unclear. In its best interest, industry should increase R&D investments toward more strategic topic areas, such as, but not limited to, those described next.

The first two technology areas examined by the Focus Area Task Force—lithography and 300 mm conversion—will be described in greater detail in section 4. The critical challenges to developing new interconnect technologies are integration of new materials and process technologies to ensure that the interconnect does not limit IC performance or functionality. Continuing improvements to manufacturing productivity may be limited unless breakthroughs are made in the density and performance of the wiring and dielectric system. In IC fabrication, transistors are fabricated near the surface of a silicon wafer, while interconnections among the transistors and to the outside world are placed on thin films deposited (and subsequently patterned and etched, etc.) on top of the silicon wafer. As lithography improves to allow smaller transistors, the maximum operating speed increases and interconnect properties become much more important. Accelerated research is required to develop low-dielectric-constant materials and processes, low-resistivity metallization processes, low-temperature processes, as well as advanced etch technologies for ultra-low damage and contamination. As circuit clock frequencies increase, aluminum metallization may be replaced by lower resistance copper, but copper is very difficult to etch. Copper also is a deep-level impurity in silicon, requiring careful processes to avoid contamination. To fully exploit the potential switching speed of the silicon transistor, the interlayer dielectric (typically a silicon dioxide with relative dielectric constant $k \approx 3.9$) also may be replaced by a material with much lower relative permittivity (lower k). Some polymers have been under investigation in this area, but much more research is required. It is clear that materials with $k < 3$ will require new manufacturing processes. Even for



thermal or deposited oxides, conventional etch technologies may be unacceptable for future technology generations because of process-induced damage and high levels of generated particulate contamination. An example of one potential candidate technology is neutral stream etch. Although still very much in the research stage, material removal by a neutral stream eliminates charge-related damage and minimizes particulate contamination while providing reasonable etch rates. Other approaches, such as high-density plasma-based systems, are in R&D as well.

The key challenge to assembly and packaging is to reduce the costs of final test, assembly, and packaging. In addition, conventional packaging technologies cannot support the expected electrical parameters of future technology generations. Packaging solutions exist for high-speed, high-performance products, but their cost is high, especially in view of the present trend toward expanding an offshore, low-cost assembly and packaging infrastructure. Although the research time horizon is near-term, an accelerated effort is required in direct-chip-attach (DCA) technologies.

In the design area, many challenges require accelerated work. Beyond the challenges of data management and overall process management, future semiconductor designers will need better tools for managing and performing system-level design, from specification, to partitioning, to synthesis. New algorithms for verification of ICs and system designs are required to make future designs tractable. Similar advances in algorithms for testability of ultra-large-scale ICs must be accelerated to meet Roadmap requirements. Because of a relatively weak infrastructure and lack of sufficient revenue, CAD companies are not likely to be able to fund the level of research necessary to advance CAD tools and technologies as set forth in the Roadmap.

SECTION 4. FOCUS AREA TECHNOLOGIES

The Council examined two technology focus areas in detail—lithography and conversion to 300 mm wafers. Lithography refers to all of the equipment and technologies necessary to transfer a pattern to the wafer, including exposure sources, tracks, photoresist, and masks. Conversion to 300 mm refers to the expected manufacturing transition from 200-mm to 300-mm-diameter wafers. The transition, or conversion, will require a new set of manufacturing tools and material handlers with highly uniform yet cost-effective processing capabilities over an area about 2.25 times larger than needed today. Each wafer in process will represent substantially greater potential revenue and net worth, so yield maximization and elimination of misprocessing, wafer breakage, and process-generated contamination will be essential. The conversion to 300 mm is expected to begin in the next 5 years at a cost possibly exceeding \$1 billion.

In the last 5 years, the U.S. semiconductor industry and semiconductor equipment supplier industry have made a significant comeback. A segment of the domestic equipment industry where this is conspicuously not the case is lithography (including photoresist and masks), further highlighting its problematic nature. This situation is perplexing, because the long-term semiconductor industry depends partly on the leadership in lithography, and lithography R&D is a fraction of total investment. DoD has long realized the importance of a viable onshore supplier of lithographic tools.

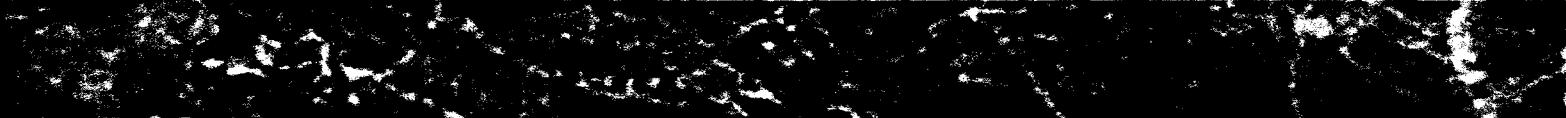
4.1 Lithography

Lithography technologies are critical to the semiconductor industry, and the Council believes that it is advisable to have competitive domestic suppliers. A coherent industry-Government strategy must be implemented and executed to accelerate R&D efforts in the most promising technology areas. SEMATECH formed an ad hoc focus area working group that also was chartered to study the options and most promising lithography technologies for the next few semiconductor generations; the group's efforts are summarized in sections 4.1.1.1–4.1.1.3. DARPA is the Government funding agency with the most extensive ongoing effort and largest projected future budget for sponsoring lithography research. The DARPA research program is evolving and increasingly emphasizing advanced lithography technologies, whereas less emphasis is placed on the infrastructure. The future direction of the DARPA research program is described in section 4.1.2.

4.1.1 R&D/Commercialization Options

4.1.1.1 Lithography Technology Options for 0.18 μm and 0.125 μm Generations

Limited R&D resources make it imperative to establish lithographic investment priorities. Optical technology is nearly certain to fulfill the requirements of the 0.18 μm generation. It now appears that enhancements to optical technology will allow extensions to the 0.125 μm generation as well. Enhancements encompass exposure tools, masks, resists, planarization, and process control. Optical technology is likely to remain the mainstream lithography choice. Exposure sources using laser-generated radiation at a 193 nm wavelength are being developed for application to the 0.18 μm technology generation.



Enhanced 193 nm technology may be applied to meet the requirements for the 0.125 μm generation as well, although there are serious challenges to producing optical elements and photoresist with sufficient properties. Geometry shrinks below 0.125 μm will be particularly challenging for 193 nm technology. As a backup option, 1x x-ray technology development should continue, with a concerted effort to solve mask issues and to increase user confidence.

4.1.1.2 Lithography Research Areas for 0.10 μm and Below Generations

Considerable uncertainty exists for the most attractive lithography technologies of 0.1 μm and below. Several large semiconductor manufacturers support 1x x-ray as a backup for the 0.125 μm technology generation with potential extendability to 0.1 μm and 0.07 μm . Again, the critical issues are x-ray source development, photoresists, and 1x masks for x-ray, including the materials, defect-free reticle production, inspection, and repair. Wider industry acceptance and involvement will be key to eventual manufacturing applications of 1x x-ray.

Extreme-ultraviolet (EUV) lithography technology also may be extendable to 0.1 μm and below. Recent advances in ultraprecise optics and precision interferometry hold promise for fabricating cost-effective aspherical optical elements. Continued research in sources of short-wavelength radiation and ultraprecise optical elements may allow production of an all-reflective lithography system at 193 nm and EUV. Production of defect-free, reflective masks is critical for EUV. Nonconventional technologies, including nonoptical approaches such as holographic lithography, charged beams, and cell projection, must be studied as potential options for exposure of features < 0.1 μm .


4.1.1.3 Required Funding Levels

The total annual development cost for lithography technologies is estimated at \$250 million, including near-term development (0.18 μm features) and long-term research, for features below 0.125 μm . Competitive analysis of foreign investments confirms the extent of required annual funding. Today, lithography R&D is being funded at about 50 percent of this level.

4.1.2 DARPA Advanced Lithography Program

The need for DoD to take the lead in information technology is manifest. Studies from the Revolution in Military Affairs to the Defense Science Board have identified information technology as the foundation of modern warfighting. DARPA recently reorganized to reflect the importance of information technology, with four out of six offices focused on that area, from R&D of large, complex systems and system demonstrations to the component information technologies.

The engine of the information revolution has been the IC, and the main issue in IC manufacturing is lithography. No other unit manufacturing technology has such a long development lead time or historically has been so problematic. Significant research funds are needed decades before a technology becomes commercially viable. Based on the recent trend of large increases in industry annual revenues, it is certainly reasonable to expect industry to be responsible for all near-term issues in semiconductor manufacturing. DARPA has been concerned about dependence on foreign



suppliers for this critical technology and has been partnering with industry in its Advanced Lithography Program. The DARPA program strategy places all responsibility for R&D investments within 5 or 6 years of production in the hands of industry, although a transition will be required from today's strategy to one in which DARPA is not involved in near-term issues.


DoD interests in lithography are closely tied to industry interests. There are some, but few, defense-unique requirements, and these generally can (and will) be integrated into the mainstream of U.S. industry needs. Although DARPA has no policy of aligning its strategy to that of industry (and in many cases must be purposefully iconoclastic to accomplish its mission), if industry is concerned about lithography dependence and its effect on assured, timely access to leading-edge manufacturing equipment, then DoD should be concerned as well. If industry is not concerned, DoD then must look hard at its own concerns because the issues are very similar. Note that optical extensions and 1x proximity x-ray are the only technologies with plausible international competition today.

The principles of the DARPA Advanced Lithography Program are as follows:

- ❖ Defense needs are the primary and overriding interest of the DARPA Advanced Lithography Program. Demonstrations of circuits should be focused on DoD applications. The goal of the DARPA Lithography Program is to ensure access to the advanced lithographic tools and materials needed to produce world-class ICs in the United States.
- ❖ The United States cannot afford, nor is it necessary to have, a defense-specific advanced lithography solution. The DARPA Advanced Lithography Program is primarily a dual-use program.
- ❖ DARPA should fund programs for successful handoff to industry. DARPA and DoD will allocate the necessary funds to execute the strategy within the President's budget, independent of congressional plus-ups. DARPA will not ask for funds above and beyond these levels and looks forward to strong industry support for an earmark-free appropriation. Creating industry buy-in in anticipation of the handoff to industry is one criterion for a successful DARPA effort. DARPA should work closely with industry leaders and industry organizations associated with lithography.
- ❖ The DARPA program should be informed of, but not controlled by, the SIA consensus position (The National Technology Roadmap for Semiconductors).
- ❖ Industry is expected to help ensure that DARPA's opportunity to hire the highest quality program managers available.
- ❖ A successful strategy must harness the growing U.S. semiconductor industry resource. Over the next 10 to 15 years, the semiconductor industry is expected to grow tenfold. The industry must determine how it will fund basic lithography research. Lithography cannot be DARPA's responsibility in perpetuity.

The goals of the DARPA Advanced Lithography Program are as follows:

- ❖ Investigate electronics manufacturing technologies for the transfer of highly complex patterns below 0.10 μm resolution over field areas exceeding 1,000 sq mm.

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- ✦ By the end of FY 97, transfer DARPA's nearer term semiconductor lithography technology R&D efforts (optical extensions and 1x proximity x-ray applicable to 0.125 μm) to industry for its continued funding or downselection.

Consistent with these goals, the DARPA Advanced Lithography Program will accomplish the following:

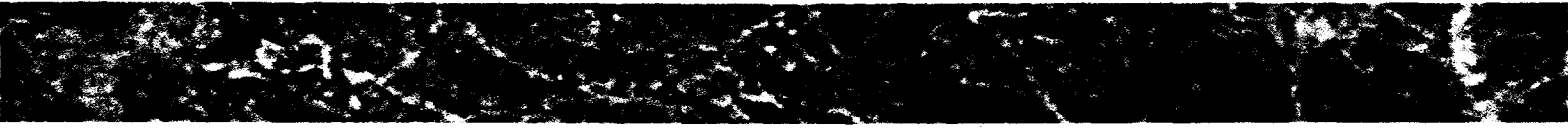
- ✦ Initiate a program to investigate electronics manufacturing technologies for the transfer of highly complex patterns below 0.10 μm resolution over field areas exceeding 1,000 sq mm.
 - Recognizing the exponentially increasing difficulty of mask write, inspect, and repair technologies, concentrate on maskless technologies with plausible manufacturing speeds.
 - Complete the FY 96 ion beam effort, at which point, a limited machine should exist to support resolution and distortion experiments. These results will be used to formulate plans for future developments of projection ion beam technology, such as complementary stencil mask technology.
- ✦ Complete, by FY 97, the optical extensions work focused on 0.18 μm and 0.125 μm .
 - Prepare a detailed roadmap of the optics options below 0.18 μm , understanding error budgets, materials, and areas needing additional breakthroughs (e.g., how would one live with a 200 nm depth of focus? How would 157 nm lasers be developed to the required maturity level in time? Are there effective sources below 157 nm? Can a robust, high-numerical-aperture, all-reflective exposure tool be built?). The purpose of this exercise is to highlight R&D areas needing investment and to aid potential downselection decisions. This study has begun.
 - Fund a limited number of critical experiments to enable data-driven decisions on optical extensions.
- ✦ Complete, by FY 97, DARPA participation in 1x proximity x-ray applicable to 0.125 μm and 0.10 μm .
 - The preponderance of these resources should go to mask issues.
 - The focus of this effort will emphasize the 0.10 μm generation unless the optics roadmap study indicates otherwise.
- ✦ Concentrate on issues of importance common to both x-ray and optical technologies for 0.125 μm feature exposure, including mask writing, mask inspection and repair, data preparation, and precision stages.
 - These areas are within scope of the DARPA FY 96-97 effort.
 - DARPA will emphasize high-throughput electron-beam writing technologies because of DoD's special needs in this area.

4.2 300 mm Conversion

Industrial conversion to a larger wafer diameter is driven solely by economics. Potentially, many more ICs may be fabricated on a larger area wafer for slightly higher processing costs (approximately 40 percent greater per-wafer processing costs). Although about \$1 billion in nonrecurrent engineering (NRE) costs are estimated to develop a 300 mm toolset, 300 mm wafers and processes will not create any new devices or unique ICs. Nontrivial technical issues certainly are associated with the scaling up and process control of specific tools and unit processes, such as plasma processes and thin-film deposition and etch. Concerns also exist for 300 mm wafer and consumable materials, but all challenges appear to be solvable through applied engineering. Great demands are placed on the equipment intended for 300 mm factories, because each wafer in process represents a much larger value than does a 200 mm wafer and thus is more important for its potential revenue. Wafer loss from mechanical breakage or misprocessing needs to be eliminated, although particulate reduction also will be important to retaining high process yields (yield is the fractional number of fully functional units per fabrication run). The timing of the demand for 300 mm tools also is of concern to suppliers, in view of high development costs and a customer base that is not unified on the issue.

Exclusive of any fundamental materials or physics research efforts, little or no reason exists for the Federal Government to fund any part of the industrial technology conversion to 300-mm-diameter wafers. Any ICs required by the DoD, including all those at the leading edge, still may be manufactured in 200 mm factories (or even 150 mm factories); the move to 300 mm wafers is strictly for industry purposes. Once the economics are favorable, industry can and should fund the entire transition. In fact, a lack of firm purchasing commitments from manufacturers has contributed to major suppliers' inactivity in large development efforts for 300 mm tools. SEMATECH is leading an effort to form an international team of companies to begin coordinating, planning, and driving the industry and suppliers on wafer conversion. Participation in the effort was solicited from U.S., European, Japanese, and other Asian companies. A second foreign effort was announced recently, a joint venture by 10 of the largest Japanese electronics companies.

In 1996, SEMATECH established the International 300 mm Initiative (I300I), a subsidiary organization with international membership. I300I is implementing a major technology and infrastructure development initiative to lead its membership and their equipment suppliers in the conversion to 300 mm diameter wafers. The objective of this initiative is to provide the driving force behind an international effort to ensure toolset availability at the appropriate time. SEMATECH's program is beginning with the development of standard short-loop structures and reprocessing, followed by 300 mm tool qualification for 0.25 μm features, multiple sourcing of tools, then 0.18 μm equipment qualification. The 300 mm subsidiary has been structured for complete separation from the regular SEMATECH program, allowing non-SEMATECH U.S. companies and foreign companies to participate in I300I without compromising the SEMATECH intellectual property developed through the regular program. With or without significant foreign participation, the SEMATECH 300 mm effort is planned to drive equipment suppliers forward and provide I300I membership with an early competitive advantage.



After several discussions with SEMATECH, the Japanese companies declined the opportunity to join I300I. Rather, 10 large Japanese electronics companies opted to organize their own effort with a broader 10-year charter to perform advanced research. The funding from member companies is about \$350 million for the first 5 years, with no decision yet on future funding. This Japanese consortium of companies—Semiconductor Leading-Edge Technologies, Inc. (SELETE)—will include efforts to solve numerous technology R&D issues for fabrication below 0.25 μm , but will emphasize 300 mm conversion. SELETE had been called Advanced Semiconductor Technologies, Inc. (ASTI) until very recently. At the time of this report, participation in the SEMATECH I300I subsidiary had been confirmed by several European and Asian (excluding Japan) firms. SEMATECH is holding discussions with SELETE to avoid duplicative efforts, identify areas of cooperation, and align both groups for quantitative measurement of semiconductor equipment performance.


SECTION 5. UNIVERSITY SEMICONDUCTOR RESEARCH STATUS AND DIRECTIONS

The Semiconductor Technology Council focused considerable discussion on the status of university research and education in the area of semiconductor manufacturing. The United States is still the world leader in semiconductor research, but corporate laboratories in Europe and Japan are investing heavily. With the retreat of corporate R&D from a fundamental toward a specific product direction, universities have emerged as a principal performer of long-term research and a critical source of technology options for the industry. Unfortunately, the costs to equip and operate a state-of-the-art clean room and processing facility have escalated to the point where it is very difficult for universities to maintain complete processing capabilities that rival those of most corporate entities.

The Council believes that a strong university research environment minimizes the long-term vulnerability of this critical industry and is essential to support the industry's long-term growth. University-based, fundamental research is critical for both the technological results and the specialized expertise it provides to students. To meet industry's projected long-term demands and growth, university-based research must be expanded in scope, stabilized in funding, and better aligned to industry's long-term requirements. The Council acknowledges the importance of the knowledge and expertise obtained by students and faculty in pursuit of research to advance industry growth.

Purchasing and operating leading-edge semiconductor equipment have become extremely expensive. For the most part, universities do not have sufficient revenue to afford these costs, especially on a 3-year perennial cycle. Leading-edge tools are meant for volume production of wafers, and their large capital costs limit their use in a research experimental environment. Development and prototype tools from equipment suppliers usually are placed at manufacturers' sites for testing and evaluation. For economic reasons, most equipment companies no longer market research-grade tools, and leading-edge production tools are meant for high-volume wafer throughput and are inappropriate for university research. Universities may find it increasingly difficult to maintain captive processing facilities capable of fabricating devices with processes that have future interest to industry. A research network (detailed in section 5.4), whether ad hoc or more formal, addresses this problem in the short term, but the difficulties of cost and logistics remain.

As discussed earlier, industry estimates for this year place a value of about \$450 million on unfunded but necessary research in specific technologies to meet NTRS requirements. Of this, at least \$150 million is suitable for university work, yet universities have capacity for only about one-third of that amount. The Council is concerned about the general state of the research equipment and experimental facilities available to most academic researchers. Because of the high costs, most universities have had difficulty in maintaining leading-edge processing capabilities, forcing many researchers to rely principally on simulations. The Government has been a major provider of funds for basic research, but even those funds are inadequate to allow institutions to purchase, operate, and maintain leading-edge processing capabilities. Simulations are certainly important as a tool, but experimental work also is required to benchmark those simulations and provide proof of principle for manufacturability. The Council believes that access to leading-edge equipment and process technology is critical for university researchers and ultimately to the industry itself.



The Council believes that expanding and improving university research and technology handoff/transfer is critical for the long-term health of the semiconductor industry. The SRC and SEMATECH, along with the Government research funding agencies, have been sponsoring efforts at academic institutions. Although the SRC and SEMATECH have coordinated reasonably well, the coordination among Government agencies and between Government and industry have not been quite as close. Without compromising the mission-directed nature of the Government R&D funding agencies, the Council believes that a new partnership between Government and industry should be formed to provide stable funding for focused university research efforts. These efforts should be jointly managed by Government and industry and should take full advantage of university creativity in blue-sky approaches, while providing general guidance on the strategic challenges facing the industry. Specific program proposals are being developed by both industry and Government, as detailed in the following sections. The Council endorses the goals of these efforts—to improve university-based semiconductor R&D and the transfer of knowledge and technology to U.S. industry.

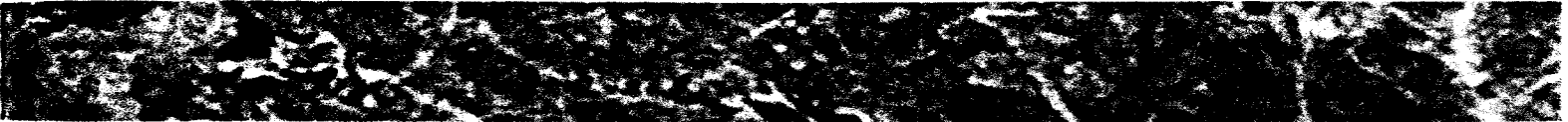
5.1 Principles in the Establishment of a University Research Initiative

Industry, Government, and academia should form a dynamic partnership, establishing a joint initiative to fund university research. An appropriate project funding, oversight, and operational framework should be adopted to accomplish the research goals and guide overall research efforts, protecting against the pressures of short-term business cycles and associated short-term needs.

The partnership should pool its resources and increase the level of funding for long-term semiconductor research by sponsoring university efforts. The funding pool should be established by a pro rata increase over the next 3 years to a minimum, stable annual budget level of at least \$60 million, provided jointly by industry and Government on a 60:40 basis. This budget will increase university funding to more than 50 percent over current levels. It is imperative that a well-defined management process for this initiative be developed and implemented. A gradual increase in the pooled budget over several years enables optimization of this management approach while stimulating research in key technology areas.

Funding under this initiative is intended for long-term strategic research (impacts well beyond 5 years) to accelerate the progress in expanding the technology options available to industry. A reasonable approach toward intellectual property and data rights should be applied up front and uniformly. Implementation of a lean management structure and process to prevent new research investments from being oriented toward shorter term goals and time horizons is necessary to preserve the initiative's strategic mission.

Most research funding under this initiative should be applied toward technologies and approaches that will meet the requirements mapped out in The National Technology Roadmap for Semiconductors. Research centers, distributed research networks, and proposals by individual investigators should be funded on a competitive basis to provide a diversity of researchers and a balance of technology approaches. About 20 percent of the total funding should be applied toward approaches not specified in the Roadmap. In either case, the



funding and research direction should not be overspecified or be linked too closely with manufacturing metrics, to protect against a shortened timeframe. Periodic project review will ensure progress, facilitate the exchange of ideas, and guide research.

5.2 Industry-Proposed Approach

The SIA sponsored an independent working group to study the issue of university research. According to that group, the implementation of the Roadmap will cost more than \$750 million in 1997, about \$450 million more than is now budgeted. Underfunded universities are being used for long-term research, while corporate R&D programs are emphasizing today's products and processes. The corporate and Federal laboratory structure that traditionally served to fill the gap between research and technology deployment is now diminishing. It was suggested that SIA members substantially increase their internal R&D budgets and also participate in creating focused university research centers.

5.2.1 Focus Center Performance Model

In the Focus Center Performance Model, each center's operations would comply with a set of goals and objectives structured to meet the technology insertion timelines of The National Technology Roadmap for Semiconductors:

- ❖ Research focus would fill the gap between long-term research and short-term technology deployment.
- ❖ The operating plan would target the solutions required for two generations out and begin to lay the foundation for third-generation insertion.
- ❖ Transfer of technology to manufacturers and suppliers would be an integral part of the operating plan.

5.2.2 Focus Center Possible Attributes

The proposed centers should be industry-driven and financially insulated from the vagaries of Federal technology policies. Moreover, the network must serve as a magnet for those firms that rely on early insertion of the most advanced manufacturing processes. Focus Center attributes would include the following:

- ❖ Nonthreatening to the traditional role of university research.
- ❖ Research largely pre-competitive, but centers could accept contracts (from suppliers) for competitive projects if such projects could help meet the center's objectives.
- ❖ Operating structure organized to compete for Federal grants on a selective basis.
- ❖ Leverage lower labor costs associated with student and postdoctoral participation, but not wholly dependent on thesis-oriented projects (i.e., some projects may have a different timescale).
- ❖ Complement current SEMATECH and SRC programs.

- ◆ Efficient transfer of work output to industry aided by industry personnel and postdoctoral researchers who want to transfer projects to industry as part of a future employment agreement.
- ◆ Intellectual property policies that promote commercial exploitation.

5.2.3 Pro Forma Funding Model for Proposed Centers

According to the SIA working group, this network could evolve up to six Focus Centers corresponding to six of the focus areas of The National Roadmap for Semiconductors. Annual funding for each center would be about \$10 million. The following is a recommended funding profile for the initiative:

◆ IC manufacturers	50%
◆ IC equipment and materials suppliers	20%
◆ Government agencies	20%
◆ Fabless companies, original equipment manufacturers (OEMs), etc.	10%

Initial capitalization could be supplemented by like-kind contributions of equipment, clean rooms, and staff.

Industry consensus is that a substantial gap exists between what industry spends today on applied research and future funding requirements to sustain industry growth. Organizations for conducting research do not have the capacity, structure, or funding required to meet Roadmap needs. A new partnership is required among all stakeholders to close the gap.

5.3 DARPA-Proposed Approach

DARPA and other R&D funding agencies share industry's concerns on the status of university research. In conjunction with other DoD agencies, and ideally with other Federal agency and industry participation as well, DARPA is developing a proposal to form a joint industry-Government research program to expand the partnership to advance semiconductor research at universities. The mission and guiding principles behind the proposed program follow.

5.3.1 The University Initiative

5.3.1.1 Mission

The mission is to establish jointly sponsored University Focus Area Initiatives as sources of expertise in vital technologies. Efforts will focus on long-term strategic challenges and, by the year 2000, will simultaneously result in the following:

- ◆ New technologies with promise for national security.
- ◆ A new mechanism to link universities (the long-term researchers) with industry (the short-term product developers).
- ◆ Twice the industry investment in strategically directed research focus areas.
- ◆ A knowledge base to enhance national security and domestic economic growth.



5.3.1.2 Environment

A new paradigm for research has emerged and is rapidly replacing the traditional approach:

- Universities are the principal performers of long-term research in the United States.
- Government agencies have mission-driven reasons to seek long-term research advantages in relevant technologies.
- Industry has reduced its long-term research investment, but needs a source for long-term product development.
- Industry has reduced the size of its in-house research laboratories and is increasing the amount of work it sends outside, while moving itself toward more applied work.
- Universities generally have favorable labor and burden rates, are on neutral ground, and employ extremely competent scientific personnel.
- Industry familiarity with university personnel provides industry insight into the best new graduates.
- Computing and communications improvements have facilitated cooperation and teaming between remote locales.

5.3.1.3 Focus Areas for the Initiatives

Focus areas include the following:

- Dual-use technologies and DoD Critical Technologies of long-term strategic importance are potential focus areas with the best chance for success under this initiative. Industry cost-sharing is required to increase the total funding for university efforts and ensure active involvement. It is desirable to solicit input from the military services and other Government agencies for technology focus areas.
- Specific centers may be established on the basis of the strengths of proposals and with concurrence from industry and Government partners. As appropriate, based on the focus area, the proposal selection criteria might include the specific technology and the research approach; potential impact of resulting research; risks; number and extent of involvement of U.S. graduate students; State, local, and university matching funds; treatment of intellectual property rights (IPR); leveraging of unfunded resources; team strength; plans for operation beyond the initiative's lifetime; and methods to accomplish research transition and information exchange.
- Once established, the centers of activity under this initiative will be funded jointly and managed by Government and industry.



5.3.1.4 Principles

The principles of the university initiative are as follows:

- ◆ Join industry, Government, and academia in a dynamic partnership to better leverage limited national resources, enhancing national security and domestic economic growth in critical industries.
- ◆ Focus on long-term research of strategic interest and the education of highly competent researchers. Long-term research is that with major impact beyond the next generation. This research addresses obstacles to products that are three technology generations, or 5 to 10 years, in the future.
- ◆ Exchange of personnel among industry, Government, and academia should be maximized through assignments, sabbaticals, mentoring, and other arrangements. Industry should find ways to reward, in terms of career advancement, company personnel assigned to the initiative's centers.
- ◆ Adopt a management oversight structure that ensures academic freedom, but encourages each partner to make the partnership succeed. Formalize treatment of the ownership of funded IPR following an industry-Government-oriented IPR approach.
- ◆ Restrict initiative funding to universities and academic institutions. Funding is intended to support the research, as well as the infrastructure and operational and maintenance costs, in performing advanced research in the focus area. Funding also may be used to partially support industrial mentors accepting assignments within the initiative's centers.
- ◆ Establish a commitment from the partnership members to share the multiyear responsibility for joint funding and management, allowing execution to the most logical points of completion.
- ◆ Coordinate and organize efforts under this initiative to complement the work of other ongoing efforts, such as industry/National Science Foundation (NSF) centers of excellence.

5.3.2 Management of the Semiconductor Research Initiative

Plans and strategies for this university-based research initiative are being formulated with the foundation that industry and Government should jointly pool additional resources (above and beyond current funding levels for semiconductor research) to fund long-term university research. This leveraged funding model is attractive because it shares risks and enhances university research capabilities. The management structure and framework for the initiative are essential to impart the initial momentum needed for success. IPR issues must be addressed up front and uniformly. Some discussion points for the initiative and its management structure follow:

- ◆ The initiative should not depend on a consensus among members for selecting or guiding projects. Disagreements will exist among the principals on the merits of any technology approach. It is more useful for the initiative to fund strategic investigations that expand the technology options available to industry.

- ❖ The time horizon of the portfolio is critical and must be actively managed by the initiative. A process needs to be instituted to eliminate substandard or near-term efforts. Figure 5-1 presents a management schema for semiconductor research.
- ❖ The National Technology Roadmap for Semiconductors lays out projected industry requirements through 2010 and provides an overall R&D framework. Most of the initiative's funding should be aligned with the Roadmap. To avoid surprises and encourage innovation, at least 20 percent of the initiative's funding should be for semiconductor research efforts that are not specified in, or lie beyond, the Roadmap.
- ❖ Only projects with potential or real payoffs beyond 5 years, and that are independent of any specific products or proprietary processes, will be considered for funding under this initiative. Other R&D in areas of interest to the semiconductor industry with a shorter timeframe may still be appropriate for universities, but should be funded by some other means. From the outset, any attempts to shorten the time horizon should be avoided.
- ❖ Initiative management must be lean and avoid project micromanagement. This approach can be implemented by using a few, very highly respected persons from the semiconductor field as managers of the initiative. To avoid micromanagement, it is critical that member institution direction for the initiative be maintained at a high level, such as director of research, chief technology officer, or a similar position.

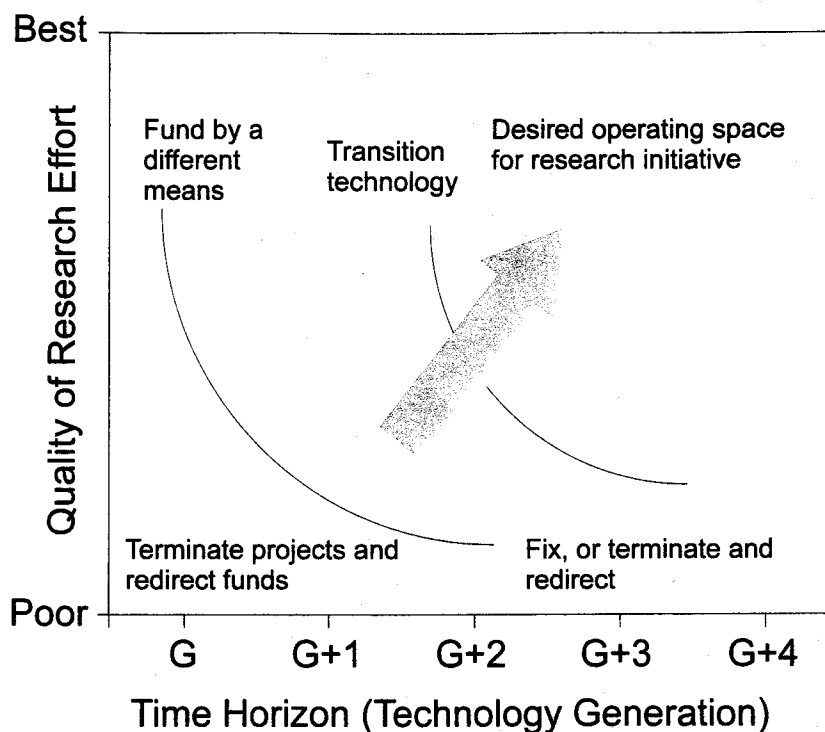
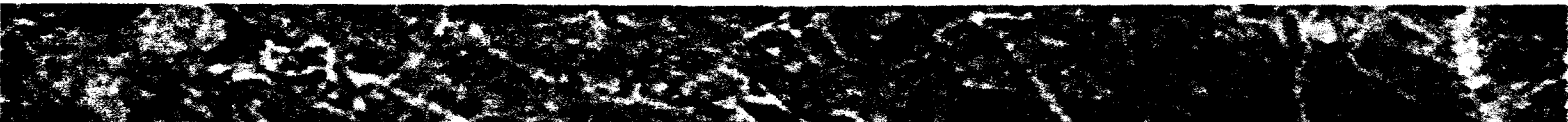


Figure 5-1. Management Schema for a University Research Initiative for Semiconductors

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- Funding for the university initiative should be “new” money, not a redirection (and subsequent reduction) from other semiconductor R&D activities.
 - All members of the initiative must have a clear view into the research programs and sponsored efforts. Active management of the initiative is well suited for encouraging and maintaining visibility into the sponsored research.

A process for IPR management must be developed and applied uniformly. The intent of this initiative is to stimulate university research and accelerate progress in technology options, not to provide the potential of future licensing fees.

5.4 University Networks of Excellence—A New Component of the Research Infrastructure


The concept of a research network consisting of several universities has been implemented in a grass-roots sense by several institutions. The research network allows universities to share resources and expertise, mitigating against the rising cost of owning fabrication equipment.

Knowledge, expertise, and capability to perform microfabrication technology research are not localized at a specific university, but distributed throughout academia. Linking university microfabrication facilities with complementary research programs will allow the transfer of wafers, processes, design rules, and research personnel, thus expanding the research capabilities of each facility. This concept is referred to as a network of excellence (NoE). As part of the overall university research infrastructure, the NoE can provide excellent education and long-range research options and solutions for transfer to focused, product-oriented development and commercialization.

The NoE concept, with efforts distributed among universities, differs greatly from the center of excellence (CoE) concept, where efforts are usually localized at one university. The institutions participating in an NoE use and expand each other's resources and resident technologies. Researchers in an NoE have access to extensive facilities, capabilities, and expertise. An NoE can provide critical-mass efforts to solve complex problems that require the complementary capabilities and expertise of several universities. Finally, an NoE approach provides a natural framework to focus the research of the participating universities.

The three cost components at any university are research, operations, and capital equipment. In most cases, Federal and industry funding organizations have concentrated on research costs rather than on operating and equipment costs. Although the NoE concept will enable academic facilities to be used more cost-efficiently, greater attention should be given to the nonresearch costs associated with maintaining and upgrading these facilities. In microfabrication, it is particularly important to keep academic capabilities current, because new industrial manufacturing technologies are introduced about every 3 years.

NoE approaches may better use distributed university resources and expertise and greatly enhance overall research capabilities. The network approach will provide excellent student and researcher education as well as exploratory research leading to solutions for critical technology challenges.



To facilitate the transfer of research to industry, it is important to develop formal coupling mechanisms and to recognize that some exploratory research areas may not have a significant industry presence yet, as was the case with MEMS-related research 20 years ago.

Although these approaches provide near-term mitigation, they do not solve the long-term issue of affordability. Capital and operational costs of maintaining leading-edge semiconductor fabrication facilities are increasing too rapidly for universities to afford such facilities for the long term. The NoE approach may be useful in some respects for one technology generation or two, but difficult problems are likely to emerge in integrating and implementing a leading-edge semiconductor manufacturing process over a wide geographical area. The long-term, strategic value of research in semiconductor processes using commercially available process modules and equipment is unclear at best. On the other hand, from a strategic viewpoint, extremely useful, leading-edge semiconductor research (and education) at universities can be realized by migrating toward laboratory, physics-based investigations of process technologies and small- to medium-scale proof-of-concept investigations. As appropriate, these investigations may be preceded by or run concurrently with theoretical or numerical modeling of the advanced technology concept. Once the physics and fundamentals have been addressed completely within the laboratory, more extensive scaling experiments may be required to better understand how laboratory results might be transferred to process equipment or modules and the potential impacts on volume manufacturing practices. In moving these new concepts from the laboratory, more sophisticated experimental work may be necessary to validate the theories of scaling, efforts that may be beyond the means of a single university in a sponsored research project. As appropriate, industrial facilities or "national" research facilities, such as the process facility at SEMATECH and the national laboratories, should be made available for university researchers to perform these experiments in a clean-room environment with the necessary infrastructure (i.e., wafers, gases, analysis tools, basic process flow, and capability). This approach would give universities access to leading-edge equipment and promote industry-academia interaction. With increased exposure, more of these concepts will be recognized, developed, and commercialized into future-generation process equipment and technologies.

SECTION 6. SUMMARY

- The long-term health of the U.S. semiconductor and equipment industries is of paramount importance. The success of previous industry and Government R&D programs and coordination is evident. Industry has turned itself around, experiencing consistent revenue and market share growth over the past few years. Many major challenges face this industry, however, and research funding must be increased, in coordination with more efficient development/commercialization activities, to meet future requirements and sustain long-term growth.
- Industry and Government are moving toward R&D funding models that are better suited to the present industrial position and capabilities. Industry is taking full responsibility for funding its mainstream infrastructure and is now planning to adapt its major cooperative R&D entities (SEMATECH and SRC) to current needs and priorities. The Government is moving the emphasis of its major semiconductor fabrication R&D investments away from infrastructure toward longer range research.
- University fabrication facilities have not kept pace with industry capabilities because of the high capital and operating expenses needed to be at the leading edge.
- Industry, Government, and academia should form a partnership, establishing a joint initiative to fund university research of strategic importance. An appropriate project funding and management framework should be implemented to accomplish the research goals and guide overall research efforts, while protecting against the pressures of short-term business cycles and associated short-term needs. The partnership should pool its resources to double the current levels of investment in university semiconductor research.
- Most research funding under this initiative should be applied toward technologies and approaches that will meet the requirements mapped out in The National Technology Roadmap for Semiconductors. Research centers, distributed research networks, and proposals by individual investigators should be funded on a competitive basis to provide a diversity of researchers and a balance of technology approaches. To encourage innovation, about 20 percent of the funding should be applied toward approaches not specified in the Roadmap. To protect against the timeframe being shortened, the funding and research direction should not be overspecified or be linked too closely with manufacturing metrics.

SECTION 7. ACKNOWLEDGMENTS

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SECTION 8. NOTES

1. This is intended as a representative list of the various types of research services available. The STC makes no endorsement of these vendors or services.
2. Status 1996, Integrated Circuit Engineering Company, Scottsdale, AZ (1996).
3. Status 1995, Integrated Circuit Engineering Company, Scottsdale, AZ (1995).
4. The National Technology Roadmap for Semiconductors, Semiconductor Industry Association (1994).