SEMATECH 1990

A REPORT TO CONGRESS BY THE ADVISORY COUNCIL ON FEDERAL PARTICIPATION IN SEMATECH

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A REPORT TO CONGRESS

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This report is submitted on behalf of the Advisory Council on Federal Participation in SEMATECH. As required by law, the report provides an assessment of the consortium's progress during its second full year of operation.

Established by the National Defense Authorization Act for Fiscal Years 1988 and 1989, and further directed by the Omnibus Trade and Competitiveness Act of 1988, the Advisory Council is charged with reviewing SEMATECH's operations each year and assessing continued federal participation.

EXECUTIVE SUMMARY

SEMATECH has become America's first large working example of an industry-led public-private partnership to promote national commercial objectives.[1] During 1989, the consortium translated its mission into operating programs, established an extensive inventory of important technology development projects, and registered substantive gains in its effort to reshape relations between U.S. chipmakers and their domestic equipment and materials suppliers. In view of these achievements and consistent with the Administration's proposed FY 1991 Budget, the Advisory Council recommends continued federal support for SEMATECH in 1991 at the current $100-million level.

DEVELOPMENTS IN SEMATECH'S OPERATING ENVIRONMENT--1989

- New Strength in the Semiconductor Industry, Continued Weakness in Supplier Industries

During 1989, several SEMATECH members including Texas Instruments (TI), Motorola, Micron, Intel and Advanced Micro Devices (AMD) took steps to reenter or expand their presence in world markets for dynamic random access memory chips (DRAMs). These developments seem to assure a continued U.S. position in world memory markets, but not a larger position. Japanese chipmakers have outspent U.S. merchant producers on new plant and equipment by 15 percent or more in every year since 1982. The margin jumped to about 60 percent ($1.7 billion) in 1988. Estimates indicate a comparable spread in 1989, with about half of Japanese spending dedicated to memory production.

The long-term prospects of SEMATECH's members were clouded during the year by continued erosion in the chipmakers' U.S.-owned supply base. Many U.S. semiconductor manufacturing equipment and materials firms are too small and cash-poor to be consistently competitive. In addition, increased foreign competition and rapidly rising R&D costs have reduced profitability and limited the capacity of supplier firms to finance continued growth from retained earnings, public stock offerings, or domestic sources of venture capital. U.S. firms in general also pay more than their foreign competitors for debt.

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[1] SEMATECH is a consortium of 14 U.S. semiconductor makers and the Department of Defense aimed at achieving global leadership in chipmaking technology by 1993. Its private members are Advanced Micro Devices, AT&T, Digital Equipment, Harris, Hewlett-Packard, Intel, IBM, LSI Logic, Micron, Motorola, National Semiconductor, NCR, Rockwell International, and Texas Instruments. The consortium's three-phased strategic plan calls for the development and demonstration of manufacturing technology for semiconductor devices with circuit dimensions of 0.8, 0.5 and 0.35 microns in 1989, 1991, and 1993 respectively. A micron is one millionth of a meter.

o **Continued Globalization**

International joint venturing by U.S. chipmakers, including the members of SEMATECH, seemed to accelerate in 1989. TI and Hitachi began marketing one another's memory products; Motorola extended its technology exchange agreement with Toshiba to 4Megabit (4Mb) DRAMs; Intel agreed to market and ultimately co-produce memory chips made by a small Japanese firm (NMB Semiconductor); and IBM joined Siemens to co-develop 64Mb DRAM product technology.[2] The globalizing trend was also apparent in direct investment by multinational firms. During 1989, at least three of Japan's leading DRAM manufacturers--NEC, Mitsubishi, and Oki--announced plans to build or expand facilities in the United States to produce 4Mb DRAMs. Similarly, many of the largest U.S. chipmakers including IBM, Digital Equipment, Motorola, and Hewlett-Packard generate major shares of their overall revenue and asset growth in overseas operations.

o **Implications**

Weakness in the Supply Base. Weakness in the U.S. semiconductor manufacturing equipment and materials industries creates a competitive vulnerability for U.S. chipmakers. Success in world semiconductor markets depends on rapid growth in production efficiency and getting to market early in the product cycle. These objectives demand close relations between the chipmakers and their suppliers including the sharing of proprietary equipment and device designs and marketing strategies, and early testing and refinement of prototype tools in production settings.

For U.S. chipmakers, however, close relations with foreign suppliers present special problems. The chipmakers report that several Japanese firms have delayed delivery of advanced equipment to American firms by two years or more. In addition, U.S. chipmakers are understandably apprehensive about sharing proprietary device designs and marketing plans with suppliers who may be linked vertically to the chipmakers' most formidable foreign rivals.

Departure by U.S. firms from the world equipment and materials market, therefore, may jeopardize the competitive position of U.S. producers in the world semiconductor market. In turn, growing dependence on foreign sources for advanced semiconductors is a potential threat to the continued competitiveness of U.S. computer and communications equipment firms and a serious problem for U.S. defense procurement. Despite diminished profit opportunities for U.S. firms in the equipment and materials industry itself, therefore, U.S. firms in downstream industries and the public at large have a common *strategic* interest in maintaining diverse sources of world-class chipmaking equipment and materials.

Globalization. Globalization in the semiconductor industry raises questions about whether and in what sense benefits of the public investment in SEMATECH can be

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[2] 4Mb DRAMs, which store 4 million bits of information, are currently the world's most advanced production DRAM chip. Only IBM and Toshiba now manufacture 4Mb DRAMs in volume.

directed to the American economy. In fact, because many SEMATECH members make and sell semiconductors in major market areas outside North America, and can be expected to use technology developed by the consortium in their overseas operations, the *direct* economic benefits of public investment in SEMATECH (e.g., jobs, tax revenues) cannot be confined to the United States. The consortium's main benefits to Americans are *indirect*. They include, for example, the economic and national security benefits that come from limiting the potential for cartels in world memory chip production and in key segments of the semiconductor manufacturing equipment and materials industry, and the benefits likely to come from the continued operation of commercially vigorous U.S.-based manufacturing firms ready and able to exploit emerging technologies.

A related concern is that joint-ventures between SEMATECH members and non-U.S. firms may negate the consortium's positive impact on the U.S. economy, first by permitting the premature release of SEMATECH-developed technology to foreign rivals, and in the long term by inviting the exploitation and absorption of the financially and technologically weaker partner. However, SEMATECH's members are well-schooled in the protection of information they consider proprietary. Moreover, in their various joint ventures with foreign firms, they are not obviously or necessarily the weaker partners.

A more challenging issue raised by the globalization of production and the emergence of complex systems of cross-national business alliances concerns the role of national policy *in general* where market developments have diluted the national identities of U.S.- and foreign-based firms. In such cases, though nations or national blocs may still vie for the benefits of global production, national policies to foster the competitiveness of domestic industries may grow more pragmatic on the issue of nationality of ownership.

SEMATECH'S PERFORMANCE IN 1989

o Adjusting Organization and Strategy

Since its founding, SEMATECH has been guided by two operating models. One of these envisions the development and demonstration of world-class manufacturing processes on-site, and the transfer of resulting technology directly to members in large, integrated, connectable chunks. The second stresses the development of leading-edge equipment and materials, chiefly by supplier firms at their home facilities, with SEMATECH's Austin fab functioning as a testing ground, and supplier sales providing the main avenue for technology transfer to U.S. chipmakers. In theory and practice, SEMATECH embraces elements of both models. During 1989, however, developing and improving U.S.-made tools and materials became the consortium's primary concern, with on-site demonstration of advanced full-flow manufacturing processes relegated to a lesser but still important status. The new priorities were evident in three key areas of the consortium's activity.

Mission. In operational terms, SEMATECH's current mission statement ("To Provide the U.S. Semiconductor Industry the Domestic Capability for World Leadership in Manufacturing") is a commitment to sustain or create at least one world-class U.S. producer in each major category of chipmaking equipment. The strategic objective for

SEMATECH's members as a group, which none has the capacity to achieve alone, is *freedom from the potential dangers of dependence on foreign sources of supply.*

To restore the commercial strength of financially pressed U.S. suppliers, improved equipment and materials must be developed *in phase with chipmakers' purchasing cycles* for the next two generations of semiconductor device technology. These cycles are reflected in the deadlines for Phases 2 and 3 of SEMATECH's R&D program--i.e., 1991 for the development of 0.5-micron production capability, and 1993 for 0.35-micron capability.

Organization and Programs. In June 1989, SEMATECH reorganized to expedite an increased volume of off-site R&D contracting. A new executive-level Investment Council reviews and approves all projects. Responsibility for contract management is vested in a large supplier relations staff. And a single engineering team, directly accountable to senior management, pushes each project from conception to conclusion.

SEMATECH assigns the highest priority and the largest share of its resources to projects aimed at averting potentially dangerous (i.e., "show-stopping") dependence on foreign suppliers for key manufacturing tools. Second highest priority goes to projects that accelerate technology development in cases where earlier access to advanced equipment, materials, or process (i.e., "key enablers") would confer a significant competitive advantage. Third place goes to high-risk/high-return projects that individual firms might not tackle on their own. In effect, these three criteria define the areas of SEMATECH's comparative advantage as a cooperative venture.

Budget. SEMATECH's current Operating Plan projects expenditures in calendar year 1990 totalling $260 million. This amount includes a sizeable carry-over from 1989. Fifty-three percent ($137 million) of the budget is earmarked for external R&D projects--up from 20 percent in 1988 and 30 percent in 1989--with roughly half of the current-year total allocated to lithography. Conversely, plant and equipment costs account for only 12 percent ($30 million) of projected 1990 spending, down substantially from 1989 when SEMATECH was still building and equipping its Austin production facility. Labor and other operating costs (e.g., fab operating costs) account for the consortium's remaining 1990 expenditures. As a result of the reallocation of spending priorities reflected in the current Operating Plan, SEMATECH's will maintain a rough 50/50 parity between internal and external expenditures during 1990 and 1991.

- <u>Developing Technology</u>

Senior officials at SEMATECH and DARPA report that the consortium's R&D program is now on track and on time. During the first part of 1989, contracting activities were slowed by differences with supplier firms on issues of intellectual property. At the end of June, only three contracts were in place. Thereafter, however, momentum increased with closure on five contracts in the third quarter, nine in the fourth, and nine more scheduled for the first three months of 1990. Contracts were concentrated in four "major thrust areas"--lithography, metrology, multilevel metalization, and manufacturing methods and processes.

During 1989, SEMATECH also demonstrated 0.8-micron manufacturing capability with 5-inch wafers at its Austin site (a basic 1989 objective) and established the generic process sequence it will use to characterize and demonstrate Phase-2 equipment and materials (i.e., 0.5-micron production capability). In September, it produced its first Phase-2 chips using Phase 2 processes with "good results."

o **Transferring Technology**

Revisions in SEMATECH's operating strategy are reflected in its approach to technology transfer. Initial (1987) planning emphasized horizontal transfers from the consortium to its members of technology developed largely on-site. Transfers to suppliers--e.g., feedback from tests of equipment prototypes--were an important but secondary concern and were confined mainly to relations between the suppliers and SEMATECH itself. The revised approach relies more heavily on two-way vertical transfers, mediated by SEMATECH but occurring with increased frequency in direct exchanges between members and suppliers.

In the most important example of the consortium's new emphasis on off-site projects and *vertical* technology exchanges, SEMATECH will buy 15-20 wafer steppers at an estimated total cost of $24 million to $32 million from GCA, a subsidiary of General Signal Corp., and consign them to five or more member companies. With technical support from GCA, members will use the machines on their own production lines, compare them to foreign alternatives, improve them, and share the resulting technology. Benefits to GCA include the revenue from the sale itself, technical feedback that should help the company to extend the shelf-life of its current stepper and improve the design of more advanced models, and the opportunity to restore customer relations that had been virtually severed.

SEMATECH has also continued to develop and apply mechanisms designed to transfer technology *horizontally*. Member-company assignees now constitute about half of the consortium's full-strength technical workforce. In addition, Austin-based technology transfer teams regularly visit member firms to assess technology needs, evaluate applications, and promote the use of SEMATECH outputs. Transfers are supported with training and technical assistance. The consortium has also hosted more than 140 visits by technical delegations from its members; convened more than 150 workshops, seminars, and advisory group sessions; circulated 200 technical documents; and formally transferred major technology packages on fab construction and 0.5-micron photoresists.

o **Improving Supplier Relations**

Historically, relations between U.S. chipmakers and their domestic suppliers have been project-specific, cost-driven, and litigious. Suppliers have borne the principal risks of product development, with relatively little customer feed-back of technical and commercial information. In contrast, SEMATECH proposes the formation of long-term cooperative relationships involving substantial and continuous cost- and information-sharing. For the chipmakers, the new pattern requires a strategic decision to cultivate local sources of supply; for the vendors, it demands a commitment to deliver world-class products on time and with extended technical support.

The consortium promotes *direct* cooperation between its members and domestic suppliers by a variety of means. The most dramatic of these are equipment improvement projects conducted at member facilities (e.g., the GCA stepper project). In a broader sense, however, SEMATECH's regimen of continuous consultation in workshops, advisory board meetings, symposia, and other forums is a means of creating the taste and talent for cooperation. In this sense, for SEMATECH, *process is outcome.*

- **Strengthening the Technology Base**

By the end of 1989, SEMATECH had established Centers of Excellence at 11 major universities (in as many states) to develop U.S. engineering talent and support the consortium's out-year R&D objectives. In addition, joint programs were under way with Sandia National Laboratory to develop reliability technology for semiconductor manufacturing equipment, and Oak Ridge National Laboratory to develop electron-cyclotron-resonance etch reactors suitable for wafer processing at 0.5-micron geometries.

IMPLICATIONS OF DEVELOPMENTS IN SEMATECH'S OPERATING STRATEGY

SEMATECH's new project-based approach mandates consensus on clearly defined R&D options and priorities. But it has also exposed a division of interest among the consortium's participants. SEMATECH's largest members already have advanced processing capability and see the consortium mainly as a way to preserve domestic sources of first-class tools and materials. In contrast, smaller members look to SEMATECH for major infusions of leading-edge process technology. The consortium's 1989 reorganization rebalanced these objectives, altering the mix of technology benefits that SEMATECH is likely to generate and testing the cohesion of the alliance. December 1989 marked the first time (under SEMATECH's 1987 Partnership Agreement) that members have been free to give the required two-year notice activating their option to leave the consortium.

SEMATECH's decision to scale back plans for in-house production may make some technology development objectives harder to achieve. Projected levels of full-flow wafer processing will be insufficient for conclusive demonstrations of equipment destined for high-volume production lines and will impose some limitation on the development of important process technologies (e.g., CIM). Moreover, generic Phase-2 and Phase-3 process architectures could omit important steps or tools that member firms would need to make their own 0.5-or 0.35-micron products. Despite these limitations, SEMATECH managers believe that the consortium's in-house production strategy will permit determination of the performance capabilities of new tools and materials with a high degree of confidence.

SEMATECH'S LIMITATIONS AS A PUBLIC INITIATIVE

Observers have suggested that SEMATECH is a "necessary but not sufficient" antidote to competitive weakness in the U.S. semiconductor industry. One reason is that the consortium's technology development efforts focus mainly on wafer processing rather than important antecedent steps (e.g., product design, materials development) or final chip assembly and packaging. In addition, SEMATECH's relatively near-term R&D objectives allow primary dependence on current-generation (i.e., optical) lithographic technology rather than X-ray and E-beam technologies that may be the basis of competitive high-volume production at the end of the 1990s.

Other factors may also affect SEMATECH's economic impact. Two of these are the financial strength and competitive tenacity of the consortium's member companies--i.e., their ability to convert technological advantage to commercial success. Others are environmental--e.g,, modest growth in the U.S. economy and in domestic markets for U.S.-made chips and chip-making gear, uncertain access to fast-growing European and Asian markets, uncompetitive U.S. capital costs, and legal and cultural barriers to domestic industrial cooperation. Aggressive application of SEMATECH's R&D outputs and improvement in these general economic conditions are both necessary, if public investment is SEMATECH is to generate high economic returns.

RECOMMENDATIONS

- <u>No Change in Funding and Oversight Responsibility</u>

DARPA's advantages as a funding and oversight agency for SEMATECH were noted in the Council's 1989 report and remain essentially unchanged--i.e., a traditional interest in "dual-use" technology, operating procedures compatible with the principle of industry leadership, a sizeable budget, a strong belief in the importance of SEMATECH's mission, and a range of existing programs that can complement or amplify the consortium's activities. In addition, DARPA has developed a close, non-intrusive, and highly productive working relationship with SEMATECH that could be difficult to replicate. These considerations argue against any shift in funding and oversight responsibility.

- <u>No Change in Current Funding Levels</u>

Consistent with the Administration FY 1991 budget proposal, the Advisory Council recommends continued federal support for SEMATECH in FY 1991 at the current $100-million level. A withdrawal or significant reduction of federal support for the consortium could seriously impair SEMATECH's ability to consolidate its recent accomplishments and move toward its Phase-2 and Phase-3 technology development goals.

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PART I

INTRODUCTION

In the past two years, SEMATECH has become America's first large working example of an industry-led public-private partnership to promote national commercial objectives.[1] Its accomplishments in 1988--defining a mission, creating an organization, building a place to work--were impressive but preparatory. They brought the consortium to the starting line with momentum, but they did not directly address its technology development agenda or the commercial and national security aims that prompted federal participation in the project. In 1989, however, SEMATECH shifted from preparation to implementation, and one could begin to assess its progress in relation to substantive goals.

As required by Congress, the chief purpose of this report is to assess SEMATECH's operations in 1989, with special attention to the extent and effect of federal participation in the project. The law reflects at least three concerns: (i) that SEMATECH should establish well-defined goals and milestones; (ii) that federal participation should not compromise industry leadership; and (iii) that regular consideration should be given to alternative methods of funding and oversight.[2]

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[1]SEMATECH is a consortium of 14 U.S. semiconductor makers and the Department of Defense aimed at achieving global leadership in semiconductor manufacturing technology by 1993. Its private members include Advanced Micro Devices, AT&T, Digital Equipment Corp., Harris Corp., Hewlett-Packard, Intel, IBM, LSI Logic, Micron Technology, Motorola, National Semiconductor, NCR, Rockwell International, and Texas Instruments. The consortium's three-phased strategic plan calls for the development and demonstration of manufacturing technology for semiconductor devices with circuit dimensions of 0.8, 0.5 and 0.35 microns in 1989, 1991, and 1993 respectively. A micron is one millionth of a meter.

[2]The following excerpt from the Council's 1989 report may be useful to readers approaching the subject of semiconductor manufacturing for the first time:

HOW MOST SEMICONDUCTORS ARE MADE

Most semiconductors are built, hundreds at a time, on thin, flat, highly polished "wafers" of ultra-pure and structurally uniform silicon. Though the order of process steps varies, basic processes and tools are common to all high-volume chip production.

- Lithography. An oxide film is deposited on each wafer, followed by a coating of light-sensitive "photoresist." Ultra-violet light focused through a glass template, or "mask," then projects minute circuit patterns on the resist. To ensure clarity, only a few copies of each image can be exposed on the resist at a time; so the projection machine, or "stepper," must move and repeat the process again and again over the entire wafer surface.

SEMATECH's experience in 1989 should allay any lingering apprehension on the first two points. The consortium has a clearer sense than it did a year ago of the operational requirements of its mission. Moreover, project oversight by DOD's Defense Advanced Projects Research Agency (DARPA) has given SEMATECH ample room for adaptation to shifting market conditions--a measure and major purpose of industry leadership in joint industry-government initiatives.

Variations in these operating patterns would be readily apparent, first because SEMATECH functions under intense and continuous public scrutiny. The consortium has been the subject of five reports to Congress and hundreds of news articles in the past year alone. A second reason is that SEMATECH is structured expressly to transfer information--e.g., through frequent on-site meetings of industry representatives and heavy reliance on assignees who communicate regularly with their home companies. These factors, and the added fact that SEMATECH is both a new cooperative entity *and* a confederation of independent businesses, give considerable assurance that developing problems--e.g., failure to meet key operating objectives or disagreement among members on tactics and strategy--will be quickly aired.

If the issues of program management and monitoring that led Congress to require this report are less problematic today than they seemed two years ago, it may be appropriate to reflect on the report's remaining purposes. One of these, certainly, is to ensure that the public perception of SEMATECH is thorough and balanced. An annual report is unlikely to bring the first news of SEMATECH's successes and failures, but it can compound or counterbalance the effect of interim and partial assessments. A second purpose is to glean SEMATECH's lessons for the design and management of other cooperative R&D initiatives. A third is to sharpen understanding of the limits of such initiatives.

- Etching. Next, the circuit patterns are developed and removed, exposing the oxide undercoating. Reactive gases or chemical solutions etch the oxide away, opening circuit paths on the surface of the silicon "substrate."

- Ion Implantation. Bombardment of the wafer surface with a high energy beam of "dopant" atoms--e.g., arsenic or boron--alters the crystal structure of the exposed silicon, raising its conductivity. To produce complex circuits, the oxidation/lithography/etch cycle is repeated as many as 20 times. Each successive circuit segment must be aligned precisely with all the rest.

- Atttaching the Circuit Contacts. Near the end of the process, a metal film is deposited and patterned to interconnect the circuit components and provide contact areas for external leads.

- Testing, Dicing, and Assembly. Once the contacts are in, an electronic probe tests each device on the wafer surface and marks defective ones with a spot of ink. Then the wafers are sliced into single chips and the inked devices discarded. Survivors are inspected microscopically, given protective casings and external leads, retested, and shipped.

THE IMPORTANCE OF HIGH-YIELD PRODUCTION

Because defective circuits cannot be identified and discarded until late in the process and wafer processing is expensive, competitive production depends on getting a high percentage of usable devices--i.e., a high "yield"--from each wafer. In early factory production of complex devices, yields can be as low as 10 or 15 percent. As manufacturing experience grows, however, yields improve to 80 percent or more.

High-yield production of advanced semiconductors requires large volumes of pure material, manufacturing atmospheres that are almost perfectly clean, and tools and processes that are precisely controlled and contamination-free. Impure material, defective photomasks, stepper misalignment, air-borne particles in the fabricating plant ("fab"), contaminants generated by the manufacturing equipment itself--anything that impairs precise imaging and etching of circuit patterns or prevents regular modification of the silicon surface in each circuit path--can ruin a chip and raise production costs.

This last purpose is central to a fair assessment of SEMATECH's achievements, but it also has a broader significance for public policy. Observers have suggested that SEMATECH is a "necessary but not sufficient" antidote to competitive decline in the U.S. semiconductor industry. The senses in which this may be true are examined below. More fundamentally, however, even at their most successful, SEMATECH and similar measures are palliatives--selective and temporary efforts to compensate for general conditions in the U.S. economy that have contributed to competitive weakness in a range of domestic industries. Barring a successful effort to alter these general conditions, SEMATECH and initiatives like it can delay but probably cannot prevent the progressive exiting of American-owned firms from research- and capital-intensive product markets.

With these purposes in view, the following sections (Parts II-V) contain a summary of major developments in SEMATECH's operating environment over the past 12 months, a review and assessment of the consortium's performance over the period, a review and assessment of federal participation in SEMATECH, and a discussion of relevant policy issues.

PART II

DEVELOPMENTS IN SEMATECH'S OPERATING ENVIRONMENT

During 1989, several SEMATECH members took steps to reenter or expand their presence in world markets for advanced dynamic random access memory chips (DRAMs). However, erosion in the market position of U.S.-owned semiconductor manufacturing equipment and materials companies seemed to accelerate.

A. DEVELOPMENTS IN THE SEMICONDUCTOR INDUSTRY--1989

(1) Slower Growth, Rising Costs

Following two banner years, growth in world-wide semiconductor sales slowed to 11 percent in 1989. Book-to-bill ratios, the industry's leading indicator, hovered well below parity for most of the year. Between July and December, waning demand and a global production glut depressed average prices on 1 Megabit (1Mb) DRAMs from $14 to $7.[1]

Private research firms project virtually static market conditions through 1990, with negative growth in the American market offset by moderately positive growth in Europe and Japan. Analysts attribute relative weakness in the American market to a sluggish macroeconomy and slack demand in a key segment of U.S. chipmakers' relatively narrow domestic customer base--i.e., the U.S. computer industry.

Softness in the world DRAM market has had varying effects on chipmakers' production plans. Five of Japan's six leading chipmakers announced plans to cut 1Mb DRAM

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[1] Electronic News (EN) (1/8/90), "Semiconductor Suppliers Gird for a Flat Year," cites data from two market research firms, VLSI Research and In-Stat. World semiconductor sales increased by 38 percent in 1988, and 23 percent in 1987. One megabit DRAMs, which store one million bits of information, are today's most advanced widely-marketed memory chips. However, IBM has been producing 4Mb DRAMs for its own use since mid-1989 and Toshiba's current plans call for high-volume production of 4Mb DRAMs for the open market in the summer of 1990. Book-to-bill ratios (compiled by the Semiconductor Industry Association of Cupertino, CA) compare the value of products shipped or billed by semiconductor firms to the value of new orders or bookings.

production by 10-17 percent in the first quarter of 1990; and Toshiba, the first Japanese firm to turn out 4Mb DRAMs in volume, has extended its schedule for "ramping up" 4Mb production from March to the summer. At least one U.S. DRAM producer, Motorola, has followed the Japanese example, delaying plans to add 1Mb production capacity. A second, Micron, is adding capacity despite falling revenues and plans to bring 4Mb DRAMs to market this summer. Korean chipmakers are also pressing ahead with plans to add 1Mb and 4Mb capacity, as is West Germany's Seimens AG.[2]

Industry experts estimate the cost of a 4Mb DRAM production facility ("fab") at more than $400 million, excluding product development costs. At the 16Mb product generation, fab costs rise to $700 million, with product development adding as much as $300 million to the total cost of market participation.[3]

(2) U.S. Firms Return to the DRAM Market

Presence in the memory market is widely considered a prerequisite for competitiveness in other areas of semiconductor production. In the past, memory production has driven the development of product and process technology in the industry at large. In addition, memory is often a component of more advanced circuits, and the ability to offer advanced memory chips in combination with more complex products (e.g., microprocessors) is a significant marketing advantage. Historically, sales of memory devices have also been an important source of revenue to support new product development. This may still be true for firms that can get to market early with high-quality products.[4] In general, however, high R&D and production costs, combined with rapidly expanding world-wide manufacturing capacity and severe market cycles, have limited the profit margins in the memory business and in the semiconductor industry at large.[5]

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[2] On Japanese and U.S. production plans, see Japan Economic Journal (JEJ) (6/17/89), "Deadheat predicted at starting gun for 4M DRAM race," and Wall Street Journal (WSJ) (1/9/90), "Japan's Biggest Memory-Chip Makers Are Cutting Output in Bid to Ease Glut." The latter article also cites Korean investment plans. In past downturns, the major Japanese chipmakers continued to add capacity and cut prices to win market share. Now, however, share is less of an issue for the Japanese who supply 70-80 percent of world demand for DRAMs. According to the New York Times (NYT) (1/18/90), "Contrasts on Chips," the major Japanese firms announced production cuts within hours of one another.

[3] On 4Mb DRAM production costs, see EN (12/11/89), "Unisys, NCR Vote No on U.S. Memories." The article reports comparable estimates by three major Japanese producers. Turner Hasty, SEMATECH's Chief Operating Officer, estimates the total cost of market entry at the 4Mb product generation at $1 billion (briefing for Commerce and DOD officials--1/11/90).

[4] WSJ (1/9/90), "Japan's Biggest Memory-Chip Makers" cites analysts' estimates that Toshiba derives 40 percent of its earnings from DRAM sales. Business Week (1/16/89), "What's Behind the Texas Instruments-Hitachi Deal," cites Pallab Chatterjee, director of TI's semiconductor process design center: "If you don't get to the market within six months of the first company, you don't make money on that entire generation of products."

[5] For much of the past decade, return on investment in the U.S. semiconductor industry as a whole has been modest in comparison with other domestic investment opportunities. A recent analysis by Dataquest, a market research firm, concluded "that the return on capital employed [long-term obligations plus stock-holders' equity] in the domestic semiconductor industry has been substandard by domestic investor expectations, while comparable returns by the Japanese and, later, the Koreans, have been acceptable to their investment constituencies" (speech by E.A. Stack, "The Role of Return on Capital Employed in the Globalization Process"). Business Week (11/13/89) reported an 11.2-percent average pre-tax return on equity for 12 leading U.S. chipmakers in the year ending 9/30/89, compared with 14.5 percent for an industry composite. On Siemens' growing market presence, see Financial Times (1/4/90),

Most U.S. merchant firms abandoned DRAM production in 1985-86 in the face of sagging global sales and fierce Japanese price-cutting. The 1986 U.S.-Japan semiconductor agreement, establishing a price floor for DRAMs, prevented a total U.S. withdrawal from the DRAM market but failed to trigger a general campaign by U.S. firms to recapture market share. In 1987, Texas Instruments (TI) and comparatively tiny Micron Corporation were the only U.S. firms still making DRAMs for the open market.

In 1989, however, several SEMATECH members took steps to reenter or expand their presence in world DRAM markets. TI broke ground for DRAM facilities in Italy and Taiwan, and committed a "significant part" of $750 million in planned 1989 capital spending to production capacity for advanced memory and logic products. Motorola, with technology licensed from Toshiba, achieved high-volume production of 1Mb DRAMs at plants in Scotland and Mesa, Arizona, and broke ground for 4Mb facilities in Sandai, Japan and Oak Hill, Texas. Micron pressed forward with plans to manufacture 4Mb DRAMs at its new Class-1 fab in Boise, Idaho, using product and process technology licensed from IBM. And Advanced Micro Devices (AMD) continued development of a submicron research and production center "to apply the manufacturing technology advances expected from SEMATECH." [6]

These developments assure a continued U.S. presence in world memory markets, but not a larger presence. Japanese chipmakers have outspent U.S. merchant producers on new plant and equipment by 15 percent or more in every year since 1982. The margin jumped to about 60 percent ($1.7 billion) in 1988; and estimates indicate a comparable spread in 1989, with about half of Japanese spending dedicated to memory production.[7]

"Philips 'risks losing lead in European chip market'."

[6] TI is now involved in a joint venture with Hitachi to share the expense and the risk of developing 16Meg DRAM product technology. Motorola returned to the DRAM market in the last quarter of 1988 with 1Meg chips manufactured at its Sandai facility. EN (1/23/89), "Motorola Plans to Build Fab for 4M DRAMs," reports that Motorola hopes to supply 4-10 percent of the overall world DRAM market in 1993. The Washington Post (Post) (11/10/89), "Future of Joint Chip Venture Now in Doubt," notes that IBM may license its 4Meg technology to Cypress Semiconductor Corp. as well as Micron. AMD's plans are detailed in the company's 1988 Annual Report (p.2). In a related development, Intel announced, in late January 1990, that it would form a U.S.-based joint venture to market DRAMs manufactured by a small Japanese firm, NMB Semiconductor. The chips will carry Intel's label, but they will be manufactured first at NMB's facilities in Japan. In return, Intel will have access to NMB manufacturing technology. Some of NMB's production may ultimately be shifted to the United States. See Post(1/23/90), "Intel Joins Japanese in Chip Deal."

[7] Dataquest estimates cited by Gary L. Guenther of the Congressional Research Service in "U.S. Semiconductor Manufacturing Equipment and Materials Industries," a memorandum to the House Science, Space, and Technology Committee (9/26/89), p. 11. Dataquest estimates that between 1986 and 1989, Japanese chipmakers increased capital spending at a 45.7 percent annual rate, compared with 28.0 percent for U.S. merchant firms (p. 23). The high rate of Japanese investment is partly a result of the recent period of high memory prices. Japanese firms supply 70-80 percent of the world memory market and 90 percent of the market for 1Mb DRAMs. High DRAM prices between 1987 and mid-1989 have been attributed to a range of causes including the 1986 U.S.-Japan semiconductor agreement and resulting supply manipulation by the Japanese. See, for example, Kenneth Flamm, "Policy and Politics in the International Semiconductor Industry," a paper presented to the SEMI ISS Seminar, Newport Beach, CA (1/16/89), p. 18: "The STA [i.e., the U.S.-Japan Semiconductor Trade Arrangement] may not have 'caused' this initial run-up in DRAM prices, in the sense that the required market power--the fact that four or five [Japanese] firms controlled 80 to 90 percent of the world merchant DRAM market--preceded the STA. But the STA appears to have been the precipitating factor which put MITI in the position of organizing and enforcing joint collusive activity on the part of these firms." See also JEJ (5/7/88), p. 10: "Japanese semiconductor industry leaders now are gradually coming to the consensus that a slight state of supply shortage will be the key to the healthy growth of the industry." On the allocation of Japanese investment, see VLSI's estimate cited in WSJ (7/24/89), "Japanese Chip Companies Brush Off U.S. Challenge and Forge Further Ahead." In 1984, 80 percent of Japanese investment went to memory production, but Japan's product focus has been shifting to more advanced chips.

(3) The Failure of U.S. Memories

U.S.Memories (USM), an ambitious seven-month campaign by four U.S. chipmakers and three systems vendors to share the costs and risks of reentering the world DRAM market, failed to generate financial support among prospective customers and closed its books in January 1990. USM planned to license IBM's 4Mb DRAM technology and to manufacture on a large enough scale to supply 4-5 percent of the world market by 1992. Financial projections assumed an initial capitalization of $500 million in shareholder equity leveraging an additional $500 million in debt.

Because USM's failure coincided with a break in DRAM prices, some observers have cited it as further evidence of short-sighted behavior in the American electronics industry at large. This judgment is probably hasty. The collapse of DRAM prices and softness in the computer market no doubt made potential shareholders more reluctant to shoulder the substantial costs of USM membership. By late 1989, however, the strategic arguments for membership had also become less compelling. Stabilization of a U.S. position in the world DRAM market and growing production capacity in Korea and Europe had reduced the potential for supply manipulation by major Japanese producers. In addition, alternatives to the creation of a new production consortium were readily available. Downstream firms interested in cost-sharing to build an independent supply base had the option of underwriting the production expenses of existing U.S. chipmakers. High-end chipmakers (e.g., Intel) needing plentiful supplies of memory chips to support full-line marketing strategies could find reliable domestic or foreign sources outside the USM framework. And even USM's most enthusiastic sponsor, IBM, could hedge its bets by licensing its 4Mb DRAM technology to other U.S. chipmakers.[8]

(4) Internationalization Continues

International joint venturing by U.S. chipmakers, including the members of SEMATECH, seemed to accelerate in 1989. TI and Hitachi began marketing one another's specialized memory products; Motorola extended its technology exchange agreement with Toshiba to 4Mb DRAMs; Intel agreed to market and ultimately co-produce NMB memory chips; and IBM joined Siemens to co-develop 64Mb DRAM product technology.[9]

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[8] USM's charter members were IBM, Hewlett-Packard, Digital Equipment, Intel, LSI Logic, National Semiconductor, and AMD. Potential U.S competitors, TI, Motorola, and Micron chose to stay outside the consortium, as did a succession of major U.S. systems makers--e.g., Sun Microsystems, NEXT, AT&T, NCR, Unysis, and Tandem. On individual cases of cost syndication see TI's 1988 Annual Report (p. 5). TI "expects to receive financial support from customers who require a strategic source of memory...." A summary judgment on USM's demise was offered by Unysis Vice President for Economic Analysis Everett Ehrlich (EN, 12/11/89, "Unysis, NCR Vote No on U.S. Memories"): "For the end-user, investing directly in any individual memory producer is only one of a number of strategies to create a more diverse and economic supply of DRAMs. It is not obvious that it has to be the preferred strategy."

[9] On the expansion of TI's cooperative arrangement with Hitachi, see WSJ ((7/21/89), "Two U.S. Makers of Chips Develop Closer Japan Ties." On Motorola's agreement with Toshiba, see JEJ (1/17/90), "Semiconductor makers ready to call a truce?" JEJ cites "10 tie-ups" between major Japanese and U.S. chipmakers "in the past year alone." The Intel-NMB arrangement is discussed in fn. 6, above. On IBM's agreement with Siemens, see Post (1/25/90), "IBM Invited Into European Chip Alliance."

In addition, senior officers of SEMATECH and JESSI, the newly established European semiconductor R&D consortium, held at least three sets of meetings--two in Austin and one in Europe--to assess options for mutual support. For now, these appear to be limited to identifying areas for complementary R&D, developing common standards for manufacturing equipment and software, and maintaining open lines of communication. The two consortia themselves are not considering cross-membership, and none of JESSI's members has applied for membership in SEMATECH.[10] In January 1990, however, IBM was invited to participate in JESSI projects.

The recent surge in cross-national partnering appears to reflect the escalating costs of world-class memory production and more traditional objectives such as access to advanced technology and fast-growing markets, and circumvention of protectionist trade policies.[11] These factors also affect direct investment by multinational firms. During 1989, for example, at least three of Japan's leading DRAM manufacturers--NEC, Oki, and Mitsubishi--announced plans to build or expand facilities in the United States to produce 4Mb DRAMs.[12] Similarly, in 1988 (the most recent year for which published data are available), many of the largest U.S. chipmakers including IBM, DEC, Motorola, and H-P generated major shares of their overall revenue and asset growth in overseas operations.[13]

(a) Implications for National Policy

Globalization in the semiconductor industry raises questions about whether and in what sense benefits of the public investment in SEMATECH can be directed to the American economy. In fact, because many SEMATECH members make and sell semiconductors

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[10] Robert Noyce, SEMATECH's Chief Executive Officer, discussed relations with JESSI in testimony to the House Science, Space and Technology Committee (11/8/89). Senior officials at SEMATECH and DARPA suggest that complementarity between the SEMATECH and JESSI research programs, combined with provisions for the timely exchange of information, would eliminate the need for cross-membership. JESSI is the acronym for Joint European Submicron Silicon. Unlike SEMATECH, JESSI has no central facility; it is primarily an agency for authorizing and funding R&D by member companies. JESSI's annual budget is nearly three times as large as SEMATECH's, but its program is broader. Its allocation for semiconductor equipment and materials R&D is roughly equal to SEMATECH's budget (conversation with DARPA Director Craig Fields--1/3/90).

[11] On trade concerns affecting the globalization of production, JEJ (1/27/90), cites MITI "guidance" to Japanese chipmakers to transfer manufacturing technology to their U.S. counterparts as "one of the best ways to calm down current U.S.-Japan chip friction." On recent revisions in the European Community's (EC) rules of origin for semiconductors, and effects of these revisions and EC local content rules on U.S. business planning see Journal of Commerce (2/7/89), "EC Announces New Chip Rules to Gain Plants"; also Financial Times (4/10/89), "U.S. chip makers fear for sales after 1992," and Post (8/2/89), U.S. Chipmakers Accuse EC of Threatening Curbs."

[12] JEJ (6/17/89), "Deadheat predicted at starting gun for 4M DRAM race"; also EN (6/19/89), "Oki Sets Oregon Fab," and "Gas Alarm Hits Mitsubishi Fab."

[13] Globalization is a major theme running through these firms' 1988 annual reports. IBM's report (p. 3), for example, notes that "moving more IBM resources close to customers is a cornerstone [of the company's recent reorganization]." Motorola's report (p. 2) observes that "the globalization of Motorola is one of the more profound trends that has been developing within the corporation over the last few years." DEC (p. 1) identifies itself as an "international company." Recent evidence, however, also indicates a counter trend. Through SEMATECH and outside licencing arrangements, for example, IBM has made a major effort to expand U.S.-owned merchant production of memory chips. Motorola may also be planning to concentrate more DRAM production capacity at U.S. sites, and has joined IBM's Fishkill, NY-based effort to use synchrotron-generated X-rays in commercial chipmaking.

in major market areas outside North America, and can be expected to use technology developed by the consortium in their overseas operations, the *direct* economic benefits of public investment in SEMATECH (e.g., jobs, tax revenues) cannot be confined to the United States. The consortium's main benefits to Americans are *indirect*. They include, for example, the economic and national security benefits that come from limiting the potential for cartels in world memory chip production and in key segments of the semiconductor manufacturing equipment and materials industry, and the benefits likely to come from the continued operation of commercially vigorous U.S.-based manufacturing firms ready and able to exploit emerging technologies.

A related concern is that joint ventures between SEMATECH members and non-U.S. firms may negate the consortium's positive impact on the U.S. economy, first by permitting the premature release of SEMATECH-developed technology to foreign rivals, and in the long term by inviting the exploitation and absorption of the financially and technologically weaker partner. As noted in the Council's 1989 report, however, SEMATECH's members are well-schooled in the protection of information they consider proprietary. Moreover, in their various joint ventures with foreign firms, they are not obviously or necessarily the weaker partners.

The globalization of production and emergence of complex systems of cross-national business alliances raises a still more challenging issue: the role of national policy *in general* where market developments have diluted the national identities of U.S.- and foreign-based firms. In such cases, though nations or national blocs may still vie for the benefits of global production, national policies to foster the competitiveness of domestic industries may grow more pragmatic on the issue of nationality of ownership. Moreover, at the enterprise level interlocking ownership may lessen incentives for nationalistic business behavior and provide a supportive environment for greater cross-national sharing of the costs and benefits of advanced applied research.[14]

B. CONDITIONS IN THE SEMICONDUCTOR MANUFACTURING EQUIPMENT AND MATERIALS INDUSTRY--EROSION CONTINUES

Despite a sharp cyclical recovery in sales in 1988, U.S. semiconductor manufacturing equipment (SME) firms as a group yielded 5 points of market share to Japanese rivals. In 1984, also a major recovery year, U.S. SME firms supplied 66 percent of world demand; by 1988, however, the U.S. share had slipped to 49.5 percent. During the same period, Japanese SME producers built their market position from 25.8 percent to 39.3 percent.[15]

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[14] Senior officials at SEMATECH and DARPA observe that the ideal of cooperation adopted by the consortium is not exclusive, and that cooperation with foreign-owned firms and foreign R&D consortia should be pursued when opportunities for mutual benefit are clear (conversations with A.S. "Obi" Oberai, SEMATECH's Director of Strategic Data & Analysis on 12/15/89, and Craig Fields on 1/3/90).

[15] VLSI Research. Some of the contrast between 1984 and 1988 reflects yen appreciation. 1988 is the last year for which data are available. Worldwide sales of wafer fabricating, assembly, and test equipment totalled $8.2 billion in 1988, $5.5 billion in 1987, and $6.1 billion in 1984.

The aggregate data mask more severe deterioration in key segments of the market. In 1988, for example, U.S. companies supplied only 22 percent of world demand for stepping aligner equipment, and U.S. positions in several important materials categories (e.g., silicon wafers) virtually disappeared. In addition, U.S. firms seem to be giving ground most rapidly at the leading edge of the market. SEMATECH companies, the primary customers for U.S.-made equipment and materials, reportedly plan to buy more than 60 percent of their processing equipment for the next two generations of semiconductor products from Japanese suppliers.[16]

Consolidation in the U.S. equipment and materials industry during the 1980s has more often been a reflection of basic weakness than gathering strength and, especially in recent years, has involved the transfer of advanced technology to foreign producers. Since 1987, the year of SEMATECH's incorporation, 65 U.S. SME and materials firms have been acquired. In 37 cases, the acquirer has been American, in 12 cases European, and in 16 cases Japanese.[17]

Three 1989 examples accent the situation of U.S. firms: (i) Huels AG's purchase of Monsanto Electric Materials Co. (MEMC), the last major U.S.-based merchant supplier of silicon wafers; (ii) Sony's acquisition of Materials Research Corp. (MRC), a major producer of sputtering equipment and thin-film materials; and (iii) Nikon's now-suspended effort to buy Perkin-Elmer's (P-E) optical lithography division. P-E, an industry leader in several key production technologies, was the world's eighth largest equipment vendor in 1988. MEMC and MRC had been on the market for long periods without attracting U.S. buyers. Similarly, P-E negotiated with Nikon after trying in vain to find an acceptable U.S. alternative. In each case, foreign buyers put a higher value on the U.S. company than the existing owners *and any potential U.S. purchaser.*[18]

The roots of the problem are systemic. Observers agree that most U.S. equipment and materials firms are too small and cash-poor to be consistently competitive. Except for

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[16] On the purchasing plans of SEMATECH members, see Bob Noyce, Testimony to the House Science, Space and Technology Committee (11/8/89). In addition, the 1989 report of the National Advisory Committee on Semiconductors (NACS) cites an industry survey indicating that "75 percent of the next generation of processing equipment purchased by U.S. companies will be produced in Japan"(p. 14). VLSI estimates that the U.S. share of world-wide equipment sales will fall another 15 points (to 35 percent) by 1993 (Guenther, p. 18).

[17] Information supplied by Sam Harrell, President of SEMI/SEMATECH, at a briefing for DOC officials (1/11/9). See also VLSI's White Paper on "The State of America's Semiconductor Equipment Industry" (November 1989), p. 4. SEMI/SEMATECH is an independent chapter of the international Semiconductor Equipment an Materials Institute limited to U.S.-owned equipment and materials vendors and established to facilitate their interaction with SEMATECH. SEMI/SEMATECH's president is a member of SEMATECH's Board. In December 1989, SEMI/SEMATECH had 142 members, down from 151 a year earlier. Housed in the SEMATECH office block, SEMI/SEMATECH now has a staff of eight. Its budget, slightly more than $1 million in 1990, is generated wholly by member subscriptions.

[18] On the MEMC sale see EN (1/23/89), "Monsanto Sale Gets U.S. OK." On MRC, see EN (8/21/89), "Sony Buying MRC for $58M In Cash Deal"; also Business Week (9/4/89), "Silicon Valley Is Watching Its Worst Nightmare Unfold." On developments surrounding the P-E sale, see EN (4/24/89), "Perkin-Elmer to Exit Semiconductor Gear"; also (12/4/89), "Nikon Halts P-E Bid; U.S. Offer Forming" and (1/6/90), "Hear SVG Bids For P-E Litho; IBM Role Seen." A pioneer in the development of photolithographic technology, P-E led the world in SME sales as recently as 1983.

a few multinational firms, U.S. vendors depend almost exclusively on a slow-growing, footloose U.S. customer base.[19] In addition, increased foreign competition and rapidly rising R&D costs have reduced profitability and limited the capacity of many U.S. firms to finance continued growth from retained earnings, public stock offerings, or domestic sources of venture capital.[20] U.S. firms in general also pay more than their foreign competitors for debt.

Like U.S. firms, foreign equipment makers face rising production costs. In other respects, however, they enjoy important advantages over most of their American rivals, including favored status in high-growth markets, close customer relations which often involve co-development of new technology, greater size and business diversity, and lower hurdle rates on prospective investments.

Weakness in the domestic supplier base creates a competitive vulnerability for U.S. chipmakers. Success in world semiconductor markets depends on rapid growth in production efficiency and getting to market early in the product cycle. These objectives demand close relations between chipmakers and their suppliers including the sharing of proprietary equipment and device designs and marketing strategies, and early testing of prototype tools in production settings.

U.S. chipmakers report, however, that several Japanese suppliers--e.g., Nikon, TEL, Kokusai--have delayed delivery of advanced equipment to American firms by two years or more. When asked at a recent industry conference whether Nikon would provide its latest and best lithography equipment to overseas chipmakers on a timely basis, Nikon Board Chairman Dr. Yoshida reportedly answered, "We will provide it, when appropriate."[21] U.S. chipmakers are also apprehensive about sharing proprietary product designs and marketing plans with suppliers who may be linked vertically to the chipmakers' most formidable foreign rivals.

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[19] Of some 850 U.S. SME and materials firms in 1988, 88 percent had sales of $25 million or less (NACS report, pp. 11-12). U.S. customers are 90 percent of the market for U.S.-made SME and materials. On erosion in the market position of U.S. chipmakers, see fn. 8, above. U.S. weakness in memory markets has been particularly damaging; VLSI calculates that each point of semiconductor market share accounted for by memory production drives a 1.4 percent share of equipment consumption (White Paper, p. 14). Dataquest estimates that Japanese chipmakers increased capital spending at an average annual rate of 45.7 percent during 1986-89, compared with a 28-percent average for U.S. merchant producers (Guenther, p. 23). In addition, much of the equipment business generated by new Korean fabs appears to be going to Japanese suppliers (EN, 3/6/89, "Korea Opportunities"). JESSI firms anticipate a 30/70 percent U.S.-Japanese split in their SME sourcing for submicron production (SEMATECH). For a salient example of footloose sourcing by U.S. companies in 1989, see EN (8/28/89), "Hear TI Lets Cannon $105M Stepper Pact."

[20] VLSI reports that R&D expenses for U.S. equipment makers rose from 5.8 percent of sales in 1979, to 16 percent in 1984, and 17.1 percent in 1987. R&D expenditures, which totalled $1.0 billion for the 1979-83 period, jumped to $2.9 billion in 1984-88. The equipment firms' five-year cumulative pre-tax income fell 40 percent between 1983 and 1988, and cumulative return on R&D declined from 76 percent in the 1979-83 period to 16 percent in 1984-88 (White Paper, pp. 9-11). Investors have been leery of U.S. equipment firms since the collapse of technology stock prices in 1985. Total public offerings by U.S. SME firms amounted to $43 million in 1985-87, compared with nearly $500 million in the previous three years, and stock prices for most firms have yet to exceed their 1983 peaks. Prospective difficulty in taking firms public has also limited the interest of U.S. venture capitalists (White Paper, pp. 7-8). SEMI/SEMATECH reports that, since mid-1987, 20 percent of its members have raised equity in Japan.

[21] SEMI/SEMATECH briefing material.

Departure by U.S. firms from the world equipment and materials market, therefore, may jeopardize U.S. prospects in the world semiconductor market. In turn, growing dependence on foreign sources for advanced semiconductors is potential threat to the continued competitiveness of U.S. computer and communications equipment firms and a serious problem for U.S. defense procurement.[22]

Despite diminished profit opportunities for U.S. firms in the equipment and materials industry itself, therefore, U.S. firms in downstream industries and the public at large have a *strategic* interest in maintaining diverse sources of world-class supply. Not even the largest downstream firms, however, have the financial strength to pursue this objective alone. In effect, many of these firms and the federal government recognized this fact when they created SEMATECH. In the past year, cultivating the U.S. supplier base has become an increasingly important feature of the consortium's operations.

C. RELATED DEVELOPMENTS

In 1989, SEMATECH was a major focus of at least two Congressionally mandated reports in addition to the first report of the Advisory Council: a report by the General Accounting Office (GAO) concluding that the consortium had made "important first steps,...[but that] more time is needed to fully measure SEMATECH's success"; and a report by the National Advisory Committee on Semiconductors (NACS) which recommended using SEMATECH to channel increased R&D support to the U.S. SME and materials industry for a period extending beyond 1993, and increasing the consortium's budget by $100 million immediately, with half of the increase provided by industry. The NACS estimated that a full-scale effort to meet the needs of U.S. equipment and materials firms would require an additional $800 million over the next three years.[23]

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[22] Commercial and national security implications of dependence on foreign suppliers for advanced semiconductors is treated at greater length in the Advisory Council's 1989 report, pp. 2-4. The national security issue gained new prominence in 1989 as a result of the publication of a new book, The Japan that Can Say "No": The New U.S.-Japan Relations Card, by Sony Board Chairman Akio Morita and Shintaro Ishihara, a prominent Japanese conservative politician. The authors suggest among other things that Japan is now in a position to alter the world military balance by supplying advanced computer chips to the Soviet Union rather than the United States (p. 3).

[23] GAO's summary assessment of SEMATECH is included in testimony by John Ols, Jr., to the House Committee on Science, Space, and Technology (11/8/89). GAO will assess SEMATECH's progress in each year that the consortium receives federal funding; its first report is entitled The SEMATECH Consortium's Start-up Activities (November 1989). The NACS recommendations are included in, A Strategic Industry At Risk (November 1989), pp. 26-27. NACS also has an annual reporting responsibility. SEMATECH's operations are also reviewed in reports by Congressional Research Service Analysts Gary L. Guenther, U.S. Semiconductor Manufacturing Equipment and Materials Industries (9/26/89), and Glenn McLoughlin, U.S. Semiconductor Equipment Manufacturers and Materials Producers (9/14/89).

PART III

SEMATECH'S PROGRESS IN 1989

In 1989, SEMATECH made an arduous transition from planning to implementation. It translated its strategic goal--creating a domestic capability for world leadership in semiconductor manufacturing--into specific operations. It established the organization and management systems to complete those operations. And it got down to the task of developing technology. In the process, it was also obliged by shifting market conditions and the logic of its own design to rebalance competing objectives and expectations.

A. MAKING THE MISSION MANAGEABLE--ALIGNING FORM AND FUNCTION

Since its founding, SEMATECH has been guided by two operating models. One of these envisions the development and demonstration of world-class manufacturing processes on-site, and the transfer of resulting technology directly to members in large, integrated, connectable chunks. The second stresses the development of leading-edge equipment and materials, chiefly by supplier firms at their home facilities, with SEMATECH's Austin fab functioning as a testing ground, and supplier sales providing the main avenue for technology transfer to U.S. chipmakers.

In theory and in practice, SEMATECH embraces elements of both models. During 1989, however, resource limitations, market developments, and other factors (e.g., the demands of internal consensus-building) affected the emphasis given to each. Developing and improving U.S.-made tools and materials became the consortium's primary concern, with on-site demonstration of advanced full-flow manufacturing processes relegated to a lesser but still important status. The new priorities were clearly reflected as SEMATECH refined its mission statement, reshaped its organization and programs, and formulated its 1990 spending plans.[1]

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[1] See the Advisory Council's 1989 report (p. 22). By the end of 1988, SEMATECH had scrapped plans for a second fab, scaled back hiring projections, and doubled its original budget for off-site R&D to 40 percent of CY 1989 spending commitments. According to Bob Noyce, SEMATECH had decided by December 1988 to shift additional resources to tools and materials development (conversation--12/11/89).

(1) Mission Statements--1988/1989

SEMATECH's mission statement as amended in June 1989 is "To Provide the U.S. Semiconductor Industry the Domestic Capability for World Leadership in Manufacturing." The current version repeats the language of its predecessor, but adds the word "domestic"--a significant clarification. Most SEMATECH members are multinational and will not confine their use of SEMATECH-generated technology to U.S. facilities. By contrast, most U.S. equipment and materials firms manufacture principally in the United States. For SEMATECH, *they* are the "domestic capability" in question, and in doubt.

In carrying out its mission, SEMATECH intends to sustain or create one world-class U.S. producer in each major category of chipmaking equipment, second-sourcing only in special cases where the back-up firm uses an entirely different tool architecture or represents a particularly high-risk/high-return investment opportunity.[2] The strategic objective for SEMATECH's members as a group, which none has the capacity to achieve alone, is *freedom from the potential dangers of dependence on foreign sources of supply.* The consortium's house flag is a modified version of a banner carried by Continental forces in the American War for Independence showing a rattlesnake coiled above the defiant warning "DONT TREAD ON ME." On SEMATECH's flag, the snake has 14 rattles.

The task of restoring independence is not only a matter of developing world-class manufacturing technology. It also involves restoring or sustaining the commercial strength of financially pressed U.S. equipment and materials suppliers. To meet the latter requirement, new or improved equipment and materials must be developed *in phase with chipmakers' purchasing cycles* for the next two generations of semiconductor device technology. These cycles are reflected in the time lines for Phases 2 and 3 of SEMATECH's R&D program, which would enable the consortium's contractors to market leading-edge equipment and materials for 0.5-micron and 0.35-micron production by late 1991 and late 1993 respectively. The world's leading memory producers have probably already made purchasing decisions for their 0.5-micron (e.g., 16Mb DRAM) fab lines. The broadest marketing window for resurgent U.S. suppliers, therefore, is likely to be at the 0.35-micron (e.g., 64Mb DRAM) product generation.[3]

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[2] Conversation with Tom Seidel, SEMATECH's Director of Manufacturing Equipment and Materials (12/14/89). Seidel is less sanguine about SEMATECH's role in rebuilding a U.S.-owned materials supply base.

[3] Observation by Turner Hasty, SEMATECH's Chief Operating Officer, to staff of the Office of Technology Assessment (OTA) (unpublished OTA trip report--5/10-12/89). The size of the marketing window for 0.5-micron equipment and materials is unclear. Not all of SEMATECH's members will need 0.5-micron production capacity in 1992. Moreover, purchasing plans at the member companies can still be changed, or additional purchases made (conversation with "Obi" Oberai--12/14/89).

(2) Refitting SEMATECH's Organization and Programs to Reflect the Mission

(a) Reorganization

SEMATECH's initial organization plan assumed that the tasks of designing, building, and operating three demonstration fab lines (one with 0.8-micron production capability, a second with 0.5-micron capability, and a third with 0.35-micron capability) would provide the framework, location, and proving ground for most of the consortium's R&D activity. This arrangement was consistent with the notion that, while SEMATECH would not produce for the market, it would function in other respects like a world-class manufacturing company.

The structure adopted by the consortium in June 1989 reflects a different vision. SEMATECH is now organized to expedite an increased volume of off-site R&D projects that meet specific equipment, materials, and manufacturing process requirements for 0.5- and 0.35-micron production. A new executive-level Investment Council reviews and approves all projects. Responsibility for contract management is vested in a large supplier relations staff. And a single engineering team, directly accountable to senior management, pushes each project from conception to conclusion.[4] The new structure incorporates a well-defined process for project definition, selection, support, and demonstration. Project-based operations also clarify staffing requirements and ensure a close fit between assignees' skills and opportunities.[5]

(b) Programs

The major ordering device in SEMATECH's project-based operating system is a Master Deliverables List (MDL) of current and potential projects. This list is based on a detailed comparison of U.S. and foreign manufacturing capabilities and the consequent targeting of "major thrust areas" for project development. For 1990, these areas include lithography, metrology, multilevel metalization, and manufacturing methods and processes.[6] The MDL currently includes 56 projects in various stages.[7] By far the largest

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[4] Minutes of the February 1989 meetings of SEMATECH's Board of Directors (Board) and Executive Technical Advisory Board (ETAB) indicate member interest in consolidating contract management responsibility and speeding up the contracting process.

[5] To further this purpose, the consortium has also established a comprehensive assignee rotation schedule. In the early part of 1989, rapid staffing and amendments in SEMATECH's program design resulted in some mismatching of assignees' expectations and opportunities. Carefully-scheduled, project-based staffing seems likely to reduce the potential for such problems.

[6] Presentation by Tom Seidel at SEMATECH's President's Day conference (12/12/89). Information for each entry in SEMATECH's first MDL (dated August 1989) includes the deliverable, the project manager, the operating goal to which the project contributes (e.g., Phase 2, Phase 3), the project schedule, and whether the project has Investment Council approval. Appended abstracts for each project include desired performance metrics (e.g., through-put, mean-time-before-failure, mean-time-to-repair, contamination limits) and an assessment of the project's effect on the competitiveness of U.S.-made equipment and materials. The deliverables list is the core SEMATECH's annually-updated Operating Plan.

number of these projects aim at developing or improving manufacturing equipment; though blocks of projects also deal with process technology (e.g., the development of diagnostic tools, sensor technology, and process control software), comparative analysis of tools and materials, and gathering or disseminating information in workshops and seminars.

SEMATECH assigns the highest priority and the largest share of its resources to projects aimed at averting potentially dangerous (i.e., "show-stopping") dependence on foreign suppliers for key manufacturing tools. Second highest priority goes to projects that accelerate technology development in cases where earlier access to advance tools, materials, or process (i.e., "key enablers") would confer a significant competitive advantage. Third place goes to high-risk/high-return projects that individual firms might not tackle on their own. In effect, these three criteria also define the areas of SEMATECH's comparative advantage as a cooperative venture.[8]

More than half the deliverables in the current MDL will be generated by Joint Development Projects (JDP)--i.e., cooperative efforts involving SEMATECH, one or more U.S. supplier companies, a federal laboratory, and/or a consortium member. A smaller, but increasing, number of deliverables are assigned to shorter-range Equipment Improvement Projects (EIP) designed to upgrade the performance and extend the competitive life of U.S.-made production equipment.[9]

Most of this work will be done off-site, with SEMATECH's Austin fab used mainly at the end of a project to demonstrate the deliverable in conditions that simulate the pressures and complexities of high-volume semiconductor production. Individual tools will be "stressed" in "short-loop" operations (i.e., by running tens of thousands of wafers through the same few process steps, using the same piece of equipment constantly until it fails) and in full-flow or "long-loop" production. SEMATECH's current plans call for a six-fold increase in fab activity (i.e., wafer moves/month) by mid-1990, with a majority of on-site effort and funding committed to short-loop operations and a significant minority committed to full-flow operations.[10]

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[7] In his 11/8/89 testimony, Bob Noyce noted 57 projects underway, of which 18 were in the definition phase, 25 in the development phase, and 14 in the demonstration phase.

[8] The MDL is reviewed by the ETAB and the Board and circulated for comment to the member companies. Its main elements, therefore, represent a consensus R&D agenda. At the margin, the consensus is always evolving. In December 1989, for example, following a zero-based budget review requested by the Board and a survey of member companies, senior management decided to deemphasize packaging and silicon materials in the consortium's 1990 program. "Show stopper" and "key enabler" are SEMATECH's own terms.

[9] Partly in response to members' advice, the EIP program has an elevated status in SEMATECH's new organization plan, and a 1990 external projects budget of about $15 million. The program will "stress" individual tools until they fail, find the cause of the failure, design a "fix," repeat the process. Some EIP projects may refine JDP outputs. Program funds may also be used to capitalize small supplier firms with promising new technologies (conversation with Larry Novak, SEMATECH's Director of Equipment Improvement and Technical Communications--12/11/89).

[10] Following a discussion of Phase 2 process architecture at its 10/18/89 meeting, SEMATECH's Board "overwhelmingly" approved this division of effort.

The consortium's Phase-1 production line, which melds 0.8-micron process technologies supplied by AT&T and IBM, will be up-graded in Phases 2 and 3 to support demonstrations of 0.5- and 0.35-micron production equipment, materials, and processes. The Phase-2 and Phase 3 lines will use generic process architecture, designed by SEMATECH and member-company engineers expressly for demonstration purposes and not to duplicate processes geared to the production of commercial devices.

(3) Reallocating Resources to Support the Mission--1990 Budget Priorities

SEMATECH's current Operating Plan projects expenditures in calendar year 1990 totalling $260 million. This amount includes a sizeable carry-over from calendar year 1989, caused by a slower-than-anticipated build-up of R&D contracting activity, and cutbacks in planned outlays for equipment and facilities as a consequence of decisions to consolidate Phase-1 production lines and cancel construction of a separate Tool Applications Process Facility (TAPF).[11]

Fifty-three percent ($137 million) of the consortium's 1990 budget is earmarked for external R&D projects--up from 20 percent in 1988 and 30 percent in 1989--with roughly half of the current-year total allocated to lithography.[12] Conversely, plant and equipment costs account for only 12 percent ($30 million) of projected 1990 spending, down substantially from 1989 when SEMATECH was still building and equipping its production facility.[13] Labor and other operating costs (e.g., fab operating costs) account for 36 percent of projected outlays in 1990 and 45 percent in 1991, though absolute spending levels are about the same in both years ($94 million and $96 million).

As a result of the reallocation of spending priorities reflected in the current Operating Plan, SEMATECH will maintain a rough 50/50 parity between internal and external expenditures during 1990 and 1991. In effect, despite increased emphasis on external projects, the consortium's management and Board have concluded that testing advanced equipment, materials, and processes in a full-flow manufacturing environment requires

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[11] Analysis of current expenditure projections suggests a 1989 carry-over of $40 million-$50 million. An additional factor contributing to the delay in SEMATECH's contracting and purchasing has been uncertainty about continued U.S. ownership of Perkin-Elmer, SEMATECH's second source for Phase-2 and Phase-3 lithography equipment. New plans for the TAPF are discussed below (p. 23).

[12] External projects include all JDPs, external EIPs, special projects, 11 university-based centers of excellence and cooperative programs at the Sandia and Oak Ridge National Laboratories. The 1988 budget projection cited here for external projects was included in the April 1988 version of SEMATECH's Operating Plan (GAO report, p. 17), and the 1989 projection was included in the December 1988 version of the Plan. The current Operating Plan envisions a decline in the "R&D Contracts" share of 1991 spending to 47 percent ($100 million on a $215-million base), in part perhaps because of absorption of the 1989 carry-over. Information on 1990 outlays for lithography programs was provided by Tom Seidel in a briefing for Commerce and DOD officials (1/1/90). SEMATECH's Annual Report (p. 18) estimates total external R&D expenditures of $38 million for CY 1989.

[13] SEMATECH spent about $75 millon on plant and equipment during the first three quarters of CY 1989, mainly to complete work on its Phase-1 fab (Annual Report, p. 18). The current Operating Plan projects a decline in combined facilities and capital equipment share of the consortium's 1991 budget to 9 percent ($19 million).

the maintenance of a substantial internal operating capability.[14]

(4) Implications

(a) For the Stability of the Alliance

SEMATECH's new project-based approach mandates consensus on clearly defined R&D options and priorities (expressed in the MDL). But it has also exposed a division of interest among the consortium's participants. SEMATECH's largest members already have advanced processing capability and see the consortium mainly as a way to preserve domestic sources of first-class tools and materials. In contrast, smaller members look to SEMATECH for major infusions of leading-edge process technology. The reorganization rebalanced these objectives, altering the mix of technology benefits that SEMATECH is likely to generate. As a result, some of the consortium's smaller firms may have reassessed their ability to support the considerable cost of membership.[15] December 1989 marked the first time (under SEMATECH's 1987 Partnership Agreement) that members have been free to give the required two-year notice activating their option to leave the alliance.

(b) For Operating Effectiveness

SEMATECH's decision to scale back plans for in-house production capacity may make some technology development objectives harder to achieve. Projected levels of full-flow wafer processing will be insufficient for conclusive demonstrations of equipment destined for high-volume production lines, and will impose some limitation on the development of important process technologies (e.g., CIM). Moreover, generic Phase-2 and Phase-3 process architectures could omit important steps or tools that member firms would need to make their own 0.5-or 0.35-micron products.[16]

Despite these limitations, SEMATECH managers believe that the consortium's in-house production strategy will permit determination of the performance capabilities of new tools and materials with a high degree of confidence.[17] They also note that the

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[14] A 50/50 split in spending priorities was proposed by management and endorsed by the Board at the December 1989 Board meeting (draft minutes).

[15] SEMATECH's annual subscription fee is one percent of previous-year semiconductor sales, with a $1-million minimum and a $15-million cap.

[16] Risks of relying on generic process architectures were discussed by Ashok Sinha, SEMATECH's Director of University and National Laboratory Programs (12/14/89). Charles Ferrell, the consortium's Director of Manufacturing Systems Development, estimates that 80 percent of the CIM software SEMATECH plans to develop could be tested in the consortium's own production facility (briefing for Commerce Department officials--1/11/90). CIM is the acronym for computer integrated manufacturing.

[17] Conversation with Tom Seidel, SEMATECH's Director for Manufacturing Equipment and Materials (12/14/89).

reorientation of SEMATECH's operating focus is not strictly a matter of choice. The consortium cannot afford to address strategic interests of the industry at large *and* install fully-integrated high-volume production lines at the same time.[18] In addition, full process integration probably requires the discipline of a product focus. To establish and operate a fully-integrated fab line, therefore, SEMATECH would have been obliged to produce some version of a saleable device, and to rely on its members to supply the necessary device and process designs (i.e., advanced proprietary technology). Whether members would have provided such support is uncertain.[19]

(c) *For the Design of Industry-Led Consortia*

SEMATECH's operational planning has always been more inclined toward the further development of existing technology than the support of new research.[20] The consortium's new emphasis on off-site projects and on the improvement of commercially available equipment probably reflect an added shortening of its operating focus. In SEMATECH's case, as noted above, the change has been dictated by the accelerated weakening of key U.S. supply capabilities. More generally, however, the tendency to shorten planning horizons appears to be a recurrent pattern in consortia exposed to market pressures.[21]

In one sense, the adjustment in SEMATECH's operating strategy seems inconsistent with a key objective of public support for cooperative R&D--i.e., to extend private investment horizons. In another, however, it fulfills a purpose implicit in the consortium's design as an *industry-led*, public-private partnership. A primary aim of industry leadership in public programs is to provide a degree of flexibility, a responsiveness to market requirements, rarely achieved by government agencies acting alone. Thus, by adapting its structure and programs to meet a severe and common problem, SEMATECH has succeeded in doing what it was designed to do.

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[18] Conversation with Bob Noyce (12/11/89). Noyce believes that to finance the construction of a fully-integrated production line, SEMATECH would have to manufacture semiconductors for the market.

[19] William Bandy, DARPA's project officer for SEMATECH, notes that process technology, in the abstract, is especially hard to develop and transfer (conversation 11/16/89). Tom Seidel discussed the problem of obtaining leading-edge product technology at a briefing for Commerce and DOD officials (1/11/90).

[20] In contrast, the consortium's strategic planning extends through the end of the century (conversation with "Obi" Oberai–12/15/89). In his 11/8/89 testimony, Bob Noyce also notes that: "Subsequent [post Phase-3] phases are being defined at SEMATECH...."

[21] For SEMATECH, these pressures are transmitted by a senior management and Board of Directors dominated by the member companies. Market pressures operate more immediately and with a similar result on Microelectronics and Computer Technology Corporation (MCC), another major research consortium that is sometimes compared with SEMATECH. MCC is almost entirely dependent on private subscriptions for its $65-million annual budget. To sustain industry support, it has been obliged to focus an increased portion of its R&D effort on small, short-term, product-oriented projects. Grant Dove, MCC's Chairman, explains the process as one in which large projects conceived by "kings" (e.g., CEOs willing to invest large sums for the long term) are finally captured by "dukes and barons" (e.g., vice presidents for R&D or product research, who have more immediate profit-and-loss objectives).

B. CONDUCTING TECHNOLOGY R&D

(1) Projects--1989

Senior officials at SEMATECH and DARPA report that the consortium's R&D program is now on track and on time.[22] During the first part of 1989, contracting activities were slowed by differences with supplier firms on issues of intellectual property and by internal organization and staffing patterns suited more to in-house than external operations.[23] At the end of June, only three contracts were in place. Thereafter, however, momentum increased with closure on five contracts in the third quarter, nine in the fourth, and nine more scheduled for the first three months of 1990.[24]

The break-through in contracting was clearly aided by SEMATECH's mid-year reorganization. An even more important aid, however, may have been increased pragmatism in the consortium's approach to issues of intellectual property. SEMATECH now negotiates the rights to jointly-developed technology (e.g., preferential purchasing and licensing rights) on a case-by-case basis, with final arrangements largely dependent on how project costs are shared and the market strength of the contractor.[25]

In January 1990, joint development and equipment improvement projects in the "major thrust areas" noted above included:

- Lithography: Contracts with GCA (a subsidiary of General Signal Corp.) of Andover, MA to develop optical wafer steppers capable of 0.5-micron and finer lithography, and to improve GCA steppers currently on the market; a contract with ATEQ Corp. of Beaverton, OR for advanced mask-making technology; and a contract with Silicon Valley Group (SVG) of Sunnyvale, CA for a new wafer conveyance or "tracking" system.

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[22] In his 11/8/89 testimony, Craig Fields noted that SEMATECH "is doing what it is supposed to do, within budget, on schedule...." At the same hearing, Bob Noyce asserted that the consortium's operating targets "are measurable and should be attainable." At a briefing for Commerce and DOD officials (1/11/90), Tom Seidel spoke of "a clear path" to Phase-3 lithography objectives, and "a high confidence factor for 1993 goals."

[23] Sam Harrell cites disagreements on intellectual property as the major cause of "gridlock" in SEMATECH's first contracting efforts (briefing for Commerce and DOD officials--1/11/90). Turner Hasty attributes some of the difficulty to structure and staffing (conversation--12/14/89). High performance standards may have been another cause of delay (observation by Tom Seidel--1/11/90).

[24] Conversation with Keith Erickson, SEMATECH's Director of Supplier Relations (12/15/89). Erickson expects the pace of contracting to ease later in 1990 (to perhaps five contracts a quarter) and then pick up again in 1992 as SEMATECH works toward its Phase-3 goals.

[25] SEMI/SEMATECH, 1988 Annual Report: "Intellectual property proved an insurmountable barrier to starting up the development contract process. In December, SEMATECH agreed to change its participation agreement to allow more flexibility in the development contract process." According to Tom Seidel, SEMATECH finances 20-40 percent of project costs; though in special cases it may assume all costs (1/11/90 briefing).

- Metrology: Contracts with KLA Instruments of Santa Clara, CA, ORASIS Corp. of Sunnyvale, and AMRAY, Inc. of Bedford, MA for high-speed high-resolution wafer defect detection systems; a contract with the National Institute of Standards and Technology (NIST) to define mask and wafer measurement standards; and a contract with Angstrom Measurements, Inc. of Sunnyvale to improve the company's scanning electron microscope.

- Multilevel Metalization: Contracts with Westech Systems, Inc. of Phoenix to develop leading-edge planarization equipment and processes;[26] Eaton Semiconductor Equipment Division of Beverly, MA for a 0.5-micron physical vapor deposition cluster tool; Lam Research of Fremont, CA to upgrade Lam's plasma metal etching system and develop new chemical vapor deposition technology; and Genus, Inc. of Mountain View, CA to modify its chemical vapor deposition system for tungsten films.

- Manufacturing Methods and Processes: Contracts with Hewlett-Packard to supply test chip masks for SEMATECH's Phase 2 processing line, and NCR Corp. for advanced isolation process technology.[27]

During 1989, SEMATECH demonstrated 0.8-micron manufacturing capability on 5-inch wafers in its Austin fab (a basic Phase-1 objective) and established the generic process sequence it will use to characterize and demonstrate Phase-2 equipment and materials. In September, it produced its first Phase-2 chips using Phase 2 processes with "good results."[28] In addition, during the year, the consortium joined with members and suppliers in in-house projects to evaluate or improve 0.5-micron photoresists, dry etch tools, rapid heating and ion implant processes, a holographic defect detection system, and an automatic wafer handling system.

(2) Implications

(a) For U.S. Leadership in Manufacturing Technology

SEMATECH could meet all of its R&D objectives on schedule and still not restore U.S. manufacturing leadership. One reason for this is the limited scope of the program

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[26] Planarization usually refers to a process in which wafers are coated (e.g., with a thin layer of glass) to round the corners of etched circuit channels, thus helping to prevent cracks in the metal overlays that connect circuit segments.

[27] On SEMATECH's contract inventory at the end of 1989, see Update SEMATECH (January 1990), "SEMATECH strengthens U.S. supplier base"; also SEMATECH Communique (December 1989); also background information included with SEMATECH's (1/9/90) press release on the CVD contract award to Lam Research; also Tom Seidel's Presidents' Day briefing on SEMATECH joint development projects (12/12/89).

[28] Turner Hasty (minutes of SEMATECH's October Board meeting). Update SEMATECH (September 1989) reports that initial runs demonstrated the operability of much of the Phase-2 process though minimum circuit dimensions on the first test chips were larger than the Phase-2 goal of 0.5 microns.

itself. SEMATECH projects focus mainly on wafer processing rather than important antecedent steps (e.g., product design, materials development) or final chip assembly and packaging. In addition, the consortium's 1991 and 1993 objectives allow primary dependence on current-generation (i.e., optical) lithography rather than X-ray and E-beam technologies that may be the basis of competitive high-volume production at the end of the 1990s. Furthermore, even if SEMATECH's R&D program is successful, U.S. chipmakers must *buy* the equipment and materials that embody the results--which means in practice that they must team with suppliers to develop and continuously improve what they buy. These activities do not follow automatically from the timely availability of advanced technology. They involve basic changes in established patterns of industry behavior.

(b) For Broader National Policy Objectives

Public investment in SEMATECH is based on a premise of substantial economic returns. Factors beyond SEMATECH's control, however, affect its ability to meet this criterion. Two of these are the financial strength and competitive tenacity of the consortium's member companies--i.e., their ability to convert technological advantage to commercial success. Other factors are environmental, for example: slow growth in the U.S. economy and in domestic markets for U.S.-made chips and chip-making gear; uncertain access to fast-growing European and Asian markets; uncompetitive U.S. capital costs; and legal and cultural barriers to domestic industrial cooperation. Aggressive application of SEMATECH's R&D outputs and improvement in these general conditions are both necessary, if public investment in SEMATECH is to generate high economic returns.

C. TRANSFERRING TECHNOLOGY

Revisions in SEMATECH's operating strategy are reflected in its approach to technology transfer. Initial planning emphasized horizontal transfers from the consortium to its members of technology developed largely on-site. Transfers to suppliers--e.g., feedback from tests of equipment prototypes--were an important but secondary concern and were confined mainly to relations between the suppliers and SEMATECH itself. The revised approach relies more heavily on two-way vertical transfers, mediated by SEMATECH but occurring with increased frequency in direct exchanges between members and suppliers.

(1) <u>Transferring Technology Horizontally</u>

Mechanisms originally designed to transfer technology from SEMATECH to its members are installed and operating. Assignees now constitute about half of SEMATECH's full-strength technical workforce. In addition, Austin-based technology transfer teams regularly visit member firms to assess technology needs, evaluate applications, and promote the use of SEMATECH outputs. Transfers are supported with training and technical assistance. The consortium has also hosted more than 140 visits by technical delegations from its members; convened more than 150 workshops, seminars, and advisory group sessions; circulated 200 technical documents; and formally transferred major technology packages on fab construction and 0.5-micron photoresists.

Finally, however, the success of SEMATECH's technology transfer effort depends on how its member companies prepare to exploit the opportunities that SEMATECH will create --e.g., whether they invest in parallel and complementary research; whether they send top-quality staff to Austin; how they position returning assignees; and whether they use the process technology and the equipment and materials that SEMATECH is helping to develop.[29]

Evidence on these points is preliminary and partial. A number of member firms seem well-positioned to use SEMATECH's R&D outputs, including at least three--TI, Intel, and AMD--who are building similar research facilities, and several (e.g., TI, Intel, and Motorola) who are adding memory production capacity.[30] Early reports indicate that member companies carefully screen candidates for assignment to SEMATECH, but the reentry experience of assignees has been uneven.[31] Six of SEMATECH's member firms will use the consortium's fab technology to build or upgrade fabs of their own.[32] And there are indications that several member companies are prepared to expand their purchasing plans to take advantage of SEMATECH-sponsored improvements in U.S.-made equipment.

(2) Transferring Technology Vertically

Some of the tool development and prototype testing originally planned for SEMATECH's TAPF will now be performed in the main fab, but the major share of such work will be assigned to the member companies.[33] In the most important of these

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[29] U.S. News & World Report (7/10/89), "High Tech's United Front," cites DEC's policy of investing a dollar on technology transfer for every dollar it invests in a consortium. A thorough treatment of this subject for SEMATECH members requires access to information on individual company plans and practices not sought for this report. GAO has flagged the subject for discussion in its own 1990 report on SEMATECH.

[30] According the companies' 1988 annual reports, TI is building a dedicated fab line for prototyping future generations of silicon-based devices including 16Mb DRAMs (p. 5); Intel has added a new facility that "will be the proving ground for memory and microcontroller process technologies" (p. 25); AMD is completing a new Submicron Development Center "to enable [it] to apply the manufacturing technology advances expected from SEMATECH" (p. 2); and Motorola has created a new Final Manufacturing R&D Center (p. 10).

[31] GAO (p. 36) describes the rigors of assignee selection; one member company screens seven applicants for every one sent to SEMATECH. Three early returnees did not fare well at one of the smaller member companies (EN (1/1/890, "SEMATECH Grads Exit AMD; Job Snag Cited"). However, returnees have been successfully reintegrated at IBM, AT&T, Motorola and TI (conversations with Turner Hasty and Ashok Sinha, SEMATECH's Director of University and National Lab Programs, on 1/11/90). Most of SEMATECH's initial assignee complement is scheduled to remain in Austin until the end of 1990.

[32] GAO, p. 35; also p. 40. Apparently, all 14 members and NSA will use aspects of the technology. SEMATECH formally transferred its fab technology in November 1988.

[33] SEMATECH's TAPF (Tool Applications Process Facility) is now the TAP (Tool Applications Program). Turner Hasty indicates that the decision to scale back the TAPF was dictated by budget priorities (briefing--12/12/89). The new arrangement has the advantage of requiring direct cooperation between chipmakers and suppliers, but it raises a difficult question about how

off-site projects, SEMATECH will buy 15-20 GCA steppers (at an estimated total cost of $24 million to $32 million) and consign them to five or more member companies. With technical support from GCA, members will use the machines on their own fab lines, compare them to foreign alternatives, improve them, and share the resulting technology. Benefits to GCA include the revenue from the sale itself, technical feedback that should help the company to extend the shelf-life of its current stepper and improve the design of more advanced models, and the opportunity to restore customer relations that had been virtually severed.[34] Rebuilding these links is essential to GCA's ability to compete continuously at the leading edge of the lithography market because much advanced lithographic technology is developed by chipmakers themselves and transferred *backward* up the production chain.

As part of its expanded equipment improvement program, SEMATECH also holds user group sessions in which members and individual suppliers assess the performance of particular pieces of equipment. Participants observe that the combined weight of customer opinion expressed in these sessions helps to overcome equipment makers' natural resistance to the idea that improvements are needed. The consortium also debriefs successful and unsuccessful bidders alike on the reasons for its contracting decisions.[35]

(3) Controlling the Transfer of Cooperative Technology

As suggested above, a premise of public participation in SEMATECH is that resulting technology will flow first to U.S. firms. Steps by the consortium to ensure this result--e.g., membership restrictions, reliance on U.S. suppliers, negotiated limits on suppliers' use of jointly developed technology--are discussed in the Council's first report (pp. 17-19, 25). In addition, during 1989, SEMATECH's Board reviewed member company procedures for safeguarding their own and SEMATECH's proprietary technology and generally concluded that the procedures are satisfactory.[36]

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information generated in members' own facilities should be shared. The arrangement does not impair SEMATECH's ability to conduct or sponsor projects that directly support its mission. However, the consortium will now undertake fewer unsolicited TAP projects, and applicants will be required to cover more of the project costs themselves.

[34] EN (3/12/90), "SEMATECH to Distribute I-liners." Members will pay installation and operating costs, and have the option to buy the improved steppers from SEMATECH at depreciated prices at the end of the project. SEMATECH's investment comprises 9-12 percent of its total budget and perhaps a quarter of all funds committed to outside projects in 1990. The impact on GCA's revenues is roughly comparable. In 1987, GCA's parent company General Signal reported revenues of $208 million from chipmaking equipment (Guenther, Table 7).

[35] SEMATECH's annual report cites four user groups held between June and September 1989 on equipment targeted for improvement projects (p. 9). SEMATECH also provides a framework for technology transfers from suppliers to their customers--e.g., the consortium's August 1989 symposium for fab managers, in which suppliers delivered papers on contamination control.

[36] On reasons for the review see EN (1/30/89), "SEMATECH Strain: Micron Hits TI-Hitachi Deal." EN (5/1/89), "SEMATECH Reviews Technology Safeguards," reports Bob Noyce's conclusion that while SEMATECH may want to revisit the issue in the future, "in general people are well satisfied with the level of protection that is given SEMATECH proprietary information."

D. STRENGTHENING THE SUPPLIER BASE

The development and dissemination of advanced manufacturing technology remains SEMATECH's most measurable and immediate objective. In pursuing this goal, however, the consortium is also systematically changing the behavior of its industry.

(1) Factors Contributing to a Stronger Supply Base

In key segments of the supply base, the immediate issue is not strength but survival--i.e., sufficient revenue in the near term to support the development of next-generation production technology. For the long term, however, the durability of the U.S. supply base requires a new regime in supplier-customer relations. Traditionally, these relations have been project-specific, cost-driven, and litigious. Suppliers have borne the principal risks of product development, with relatively little customer feed-back of technical and commercial information. In contrast, SEMATECH proposes the formation of long-term cooperative relationships involving substantial and continuous cost- and information-sharing. For the chipmakers, the new pattern requires a strategic decision to cultivate local sources of supply; for the vendors, it demands a commitment to deliver world-class products on time and with extended technical support.[37]

(2) SEMATECH's Approach

(a) To Financial Difficulties in the Supplier Industry

Observers contend that SEMATECH's total budget for external projects ($137 million in 1990, declining to $100 million in 1991) falls so far short of total estimated development costs for the next generation of chipmaking tools (perhaps $2.5 billion), that the consortium cannot hope to solve the financial problems of the supplier industry at large.[38] However, the contrast has limited significance for an assessment of SEMATECH's ability to accomplish the strategic goal of preserving world-class supply capability in key segments of the industry. The consortium's financial resources may indeed be proportionate to that more limited purpose.

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[37] On the benefits of strategic relationships between chipmakers and their suppliers, see VLSI, op. cit., pp. 12-13: "We believe Japan will soon surpass the United States in worldwide market share based on current trends. The primary reason for this shift is....[that] in Japan, customers show a high degree of commitment to their vendors."

[38] VLSI, op. cit., p. 15. The NACS report (p. 12) cites a preliminary analysis by Semiconductor Equipment and Materials International indicating that $1.2 billion will be required over the next three years to restore the health of the U.S. supplier base.

(b) To Supplier-Customer Relations

SEMATECH's efforts to build cooperative relations with its own suppliers--e.g., by establishing a large supplier relations staff and well-defined contract procedures--are detailed above. The consortium also promotes *direct* cooperation between its members and domestic suppliers by a variety of means. The most dramatic of these are equipment improvement projects conducted at member facilities (e.g., the GCA stepper project). In addition, SEMATECH has established a council of senior purchasing and material managers from each of its members to champion strategic relations with U.S. suppliers at their home companies.[39]

In a broader sense, however, SEMATECH's regimen of continuous consultation in workshops, user groups, advisory board meetings, symposia, joint sessions of the SEMATECH and SEMI/SEMATECH Boards, and other forums is a means of creating the taste and talent for independent cooperation. In this sense, for SEMATECH, *process is outcome.*[40]

(c) To Consolidation in the Supplier Base

SEMATECH also seeks to influence the pace and character of continuing consolidation in the semiconductor industry's domestic supply base. The consortium's mission statement and contracting practices acknowledge implicitly that key segments of the U.S. equipment and materials market can support only one or a few strong vendors.[41] In addition, SEMATECH actively encourages teaming among potential contractors and will develop equipment compatibility standards as a technical basis for increased vendor cooperation. In a few cases involving divestitures of strategically important supplier companies (e.g., MEMC and Perkin-Elmer), SEMATECH has also supported efforts by domestic firms to structure acceptable acquisition plans. [42]

[39] Established in June 1989, the Supplier Relations Action Council (also called "the partnering posse") is also charged with developing common supplier-relations guidelines and generic total quality and cost management processes (discussion with Keith Erickson--12/15/89).

[40] The SEMATECH and SEMI/SEMATECH Boards meet in joint session every quarter. Through the end of 1989, there had been 66 "one-on-one" meetings between SEMATECH and supplier-company executives, 40 workshops, nearly 150 site visits to SEMATECH by suppliers (briefing by Sam Harrell--1/11/90).

[41] EN (3\12\90), "SEMATECH to Distribute I-Liners" cites Keith Erickson's explanation of the considerations underlying the GCA equipment improvement project: "They [the consortium's competitive analysis group] look at how many companies can realistically survive in a given sector." Asked whether the GCA effort meant that SEMATECH was turning its back on the few alternative U.S. lithographic equipment suppliers, Erickson replied "There's no doubt about it."

[42] Conversation Sam Harrell (11/15/88) on SEMATECH's effort to find a U.S. buyer for MEMC; briefing by Turner Hasty (1/11/90) on SEMATECH's encouragement of efforts by U.S. firms to acquire P-E's optical lithography and E-beam divisions. MEMC was ultimately acquired by Huels AG of West Germany. A coalition of U.S. firms including IBM and DuPont recently purchased P-E's E-beam division, and a second group including IBM and Silicon Valley Group are reportedly negotiating to purchase P-E's optical lithography division (Post, 3/20/90, "U.S. Firms Team Up to Buy Chip Equipment Business"). Nikon had been an early suitor for both divisions (EN, 12/4/89, "Nikon Halts P-E Bid; U.S. Offer Forming?").

(3) Results

Advances achieved in supplier relations through much of 1989 were limited primarily to SEMATECH's own projects and the interactions of senior executives of member and supplier companies within the SEMATECH framework. In many of the member companies, top management's recognition of the need for strategic partnership had not been translated into commitment at the operating level (i.e., among purchasing officers and manufacturing managers). At yearend, however, major changes in this pattern had begun to appear.

The consortium's special stepper project, in particular, is a major exploratory step by several of SEMATECH's larger members toward a general policy of long-term cooperation with domestic suppliers. In addition, SEMATECH members who source overseas have expressed a willingness to share information with domestic suppliers on the performance of foreign-made tools and materials. A new degree of cooperation is also apparent in the joint effort of U.S. chipmakers and suppliers to acquire Perkin-Elmer's E-beam and optical lithography divisions.

SEMATECH's effort to promote cooperation among its own suppliers has produced at least one notable result--a joint agreement by three companies to supply ultra-pure gases to the Austin fab.[43] In a related development that tracks SEMATECH's own work on common standards, a number of U.S. equipment makers have launched a joint effort to generate common specifications for cluster tools.[44]

E. STRENGTHENING THE TECHNOLOGY BASE

SEMATECH's two-part apparatus for strengthening the semiconductor industry's domestic technology base involves SEMATECH Centers of Excellence (SCOE) at major U.S. universities, and arrangements to enlist the technical resources of selected national laboratories (NL). As 1990 began, this apparatus--including 11 SCOEs and two NL technical assistance agreements--was largely installed and functioning.[45]

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[43] Each of the companies, Semi-Gas, Union Carbide, and Wilson Oxygen specializes in a different phase of the delivery process--i.e., production, filtration, or distribution.

[44] The Modular Equipment Standards Architecture (MESA) group was established in December 1988 and now includes at least 25 U.S. companies, several of whom are SEMATECH contractors. In September 1989, MESA became part of Semiconductor Equipment and Materials International's (SEMI) international standard-setting activity.

[45] SEMATECH's SCOE program is administered by the Semiconductor Research Corporation (SRC), a consortium supported mainly by U.S. chipmakers to promote generic semiconductor research at U.S. universities. In 1989, SRC funded research by over 500 graduate students at more than 45 universities. Its budget was roughly $30 million, including $10 million provided by SEMATECH for the SCOEs and $2.4 million from federal agencies. The SCOEs and SRC are discussed in more detail in last year's ACFPS report. Information on SRC's 1989 operations is based on testimony provided by the organization's president, Larry Sumney, to subcommittees of the House Science, Space and Technology Committee (11/8/89). SEMATECH funds and manages its arrangements with Sandia and Oak Ridge National Laboratories separately and directly.

(1) The SCOEs and SEMATECH's Manufacturing Specialist Program

SCOEs have now been established at university facilities in Arizona, California, Florida, Massachusetts, New Jersey, New Mexico, New York, North Carolina, Pennsylvania, Texas and Wisconsin. Institutional participation in most centers includes more than one university and in some cases a federal laboratory. SEMATECH's budget for university-based SCOEs has remained roughly constant at $10 million and no additional centers are currently planned.[46]

SCOE research outputs are not expected to have a major impact on SEMATECH's near-term R&D objectives. The program's primary aim is to add to the pool of home-grown talent in manufacturing engineering. Nonetheless, SEMATECH's investment in the SCOEs has generated some early unanticipated returns in the form of improved scientific understanding (4 cases), new experimental capability (6 cases), and new product concepts (7 cases).[47]

SEMATECH has also established a training program for manufacturing technicians. As of December 1989, more than 75 SEMATECH employees had completed this course. Together with the graduates themselves, SEMATECH is likely to be the principal immediate beneficiary of the program. In time, however, trainees will move on, adding to the quality of the labor force in the industry at large.[48]

(2) SEMATECH's National Laboratory Programs

In August 1989, SEMATECH reached agreement with Sandia National Laboratory to establish a Semiconductor Equipment Technology Center (SETEC) at the lab's Albuquerque facility. SETEC applies Sandia's expertise in nuclear power and weapons reliability to the development of reliability technology for semiconductor manufacturing equipment--e.g., equipment design methodologies, new sensors and diagnostic methods, and improvements in the reliability of existing tools. The new Center is also supporting SEMATECH's joint projects with GCA and Eaton, and is likely to participate in two equipment improvement programs now in the final planning stage. The consortium will commit $10 million to SETEC's budget over the next three years.[49]

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[46] SEMATECH's Annual Report (pp. 7, 20-25) provides a thorough summary of SEMATECH's SCOE program, including locations, participants, research agendas, and 1989 accomplishments.

[47] Presentation by Ashok Sinha on SEMATECH's university and national lab programs (12/11/89). SEMATECH terms these early results "nuggets." Sinha also noted that the SCOEs have begun to graduate their first two-year Masters Degree students.

[48] SEMATECH, Annual Report, pp. 10-11. SEMATECH is exploring options for the development of a model semiconductor curriculum. Turner Hasty cited the shortage of skilled fab technicians as a significant obstacle to the rapid expansion of U.S. semiconductor production capacity (1/11/89 briefing).

[49] Briefing by Ashok Sinha (1/11/90); also Update SEMATECH (November 1989), "SEMATECH, Sandia to develop national tool design center."

In December, SEMATECH also announced a joint program at Oak Ridge National Laboratory (Oak Ridge, TN), using the lab's expertise in plasma containment and diagnostics for fusion research to develop electron-cyclotron-resonance etch reactors suitable for wafer processing at 0.5-micron geometries. The lab will evaluate several etch concepts; then SEMATECH will select the best configuration and transfer the technology to a U.S. tool maker.[50]

SEMATECH continues to seek opportunities to apply the technical resources of the national laboratories to advanced chipmaking. It has vested responsibility to identify and exploit such opportunities in a Manager for National Lab Programs, and plans to bring all lab project directors working in areas important to SEMATECH to Austin in March for a day-long conference.[51]

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[50] SEMATECH news release (12/20/89); also SEMATECH, Annual Report (pp. 5, 19).

[51] Conversation with Ron Horwath, SEMATECH's Manager for National Lab Programs (3/7/90). The March workshop will update the reviews conducted at two 1987 workshops sponsored by the National Research Council on the semiconductor industry an the national labs. The proceedings of these workshops, The Semiconductor Industry and the National Laboratories and DOE National Laboratories and the Semiconductor Industry: Continuing the Joint Planning, were published in 1987 by the National Academy Press.

PART IV

FEDERAL PARTICIPATION IN SEMATECH: DESCRIPTION AND ASSESSMENT

SEMATECH's main institutional contact points at the federal level during 1989 were DARPA and the National Security Agency (NSA), selected DOE national labs, and the Commerce Department's National Institute of Standards and Technology (NIST).

A. DOD--DARPA AND NSA

Early concerns about DOD oversight and funding of SEMATECH focused on two potential problems: (i) that SEMATECH's economic objectives might be subordinated to more limited national security interests; and (ii) that federal micro-management might limit SEMATECH's flexibility in the face of shifting market conditions.

In general, however, DARPA has not pressed SEMATECH to extend its mission beyond the limits defined by the consortium itself as consistent with its resources and the common interests of the member companies. Rather, DARPA officials have emphasized the need for complementary R&D efforts--e.g., in the areas of semiconductor product design, advanced materials, X-ray lithography, and computer integrated manufacturing--and have taken pains to keep SEMATECH well-informed about the agency's own programs in these areas. Bob Noyce expressed SEMATECH's appreciation of DARPA's contributions in recent testimony. "I can unequivocally state," he said, "that DARPA has been an intelligent, dedicated and helpful partner."[1]

In addition, during 1989, SEMATECH developed a more extensive and continuous

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[1] Hearings by joint subcommittees of the House Science, Space and Technology Committee (11/8/89). On DARPA's technology support role, Craig Fields observed at the same hearing that his agency's "value added goes beyond funding...perhaps most importantly [to] transitioning to SEMATECH other semiconductor technology supported by DARPA." William Bandy, DARPA's project officer for SEMATECH, considers it a major part of his job to keep the consortium informed about related DARPA research programs (conversation on 11/22/89). DARPA program managers briefed SEMATECH staff on these activities at a June 29, 1989 meeting.

working relationship with NSA's internal microelectronics group. Technology developed by SEMATECH has been applied in the construction of NSA's new chip fabricating plant and SEMATECH-developed equipment may be used at the Agency's main test facility.[2]

B. THE DOE NATIONAL LABORATORIES

In recent years, legislation and departmental policy have opened opportunities for DOE's national laboratories to expand their traditional focus on basic science and defense technology to include support for national economic objectives. The labs seem especially well equipped to play a larger role in the development of semiconductor manufacturing technology. In general, however, their participation in SEMATECH projects has been limited and slow to develop.[3]

During 1989, senior officers at SEMATECH expressed frustration at the pace of negotiations with the national labs on joint research initiatives. Observers attribute the problem to several factors. Bob Noyce, for example, cites a need for top-down implementation of an expanded set of operating objectives for the labs. Others have suggested practical adjustments--e.g., increased flexibility on intellectual property issues; the creation of mechanisms for informal cooperation with outsiders; and increased encouragement of laboratory staff to commercialize their work. Others point to a need for more persistent efforts by private industry to mine the labs' commercial potential.[4]

Despite these problems, as noted above, SEMATECH established promising joint research programs during 1989 at the Sandia and Oak Ridge, and continues to seek opportunities for cooperation within the national laboratory system.

C. NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

NIST, as the leading national laboratory for providing measurements, has worked closely with the semiconductor industry for many years on metrological problems and is well positioned to collaborate with SEMATECH. During 1989, NIST's involvement in

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[2] Conversation with Bill Bandy (5/3/90).

[3] The Technology Transfer Act of 1986 frees the labs to enter joint ventures with individual private firms or consortia. In addition, the legislation creating SEMATECH explicitly directs the Secretary of Energy to establish a national lab "Initiative" to support the consortium's objectives (P.L. 100-180, Part D). On the labs' potential to support semiconductor R&D, see proceedings of the NRC workshops cited in Part II, fn. 51, above. Participants in the workshops included senior managers of the national labs themselves. GAO's 1989 report (p. 33) takes note of the labs' "limited" participation in SEMATECH's long-term R&D program.

[4] Interview for this report (12/11/89). Ways to increase the labs' accessibility to private industry were discussed in a recent meeting of the Federal Laboratory Consortium for Technology Transfer (Ashok Sinha--12/13/89). Intellectual property issues delayed SEMATECH's joint project at Oak Ridge. Some observers suggest that Japanese firms have been more persistent and more succesful than their U.S. counterparts in dealing with the labs.

SEMATECH-sponsored R&D was limited to a single project in lithographic metrology. As 1990 began, however, the pace of cooperative activity quickened. NIST and SEMATECH signed a basic cooperative R&D agreement which will protect SEMATECH's proprietary interest in technology developed in NIST-SEMATECH projects. In addition, SEMATECH's Investment Council authorized consortium support for two additional NIST projects--one to characterize a standard experimental chamber for plasma processing and diagnostic tools, and a second to continue the lithographic measurement work begun in 1989. SEMATECH's financial contributions to these two projects total about $750 thousand.[5]

[5] Conversation with Robert Scace, Deputy Director of the NIST Center for Electronics and Electrical Engineering (3/27/90).

PART V

RECOMMENDATIONS

The Council supports the Administration's FY 1991 budget decision to continue funding SEMATECH, through DARPA, at the current rate of $100 million/year.

A. NO CHANGE IN OVERSIGHT RESPONSIBILITY

DARPA's advantages as a oversight and funding agency for SEMATECH were noted in the Council's 1989 report and remain essentially unchanged--i.e., a traditional interest in "dual-use" technology, operating procedures compatible with the principle of industry leadership, a sizeable budget, a strong belief in the importance of SEMATECH's mission, and a range of existing programs that can complement or amplify the consortium's activities. In addition, DARPA has developed a close, non-intrusive, and highly productive working relationship with SEMATECH that could be difficult to replicate.

As the 1989 report also noted, though DOE and NIST now have the authority and technical resources to take on DARPA's SEMATECH-related duties, neither agency could do so in practice without a larger budget and difficult adjustments in priorities, procedures, and staffing. However, the recent funding of NIST's Advanced Technology Program (at $10 million in FY 1990) has made cooperation between DARPA and NIST on SEMATECH and similar initiatives more likely in the future.

B. NO CHANGE IN THE LEVEL OF FEDERAL FUNDING

Four general options have been proposed for the federal contribution to SEMATECH's budget. Two of these, reportedly considered in the course of Administration deliberations on the FY 1991 defense budget, are: (i) to cancel or curtail federal financial participation in SEMATECH; or (ii) to maintain current levels of federal investment in the program. Two further options implied by the 1989 NACS report are: (iii) to increase SEMATECH's budget substantially at once (e.g., by $100 provided jointly by industry and government); and (iv) to increase such funding by a much larger amount (perhaps $800 million) over the next three years. The Council recommends option (ii) for the reasons discussed below.

(1) Cancelling or Curtailing Federal Participation

SEMATECH is now a major concentration of disciplined capacity to drive and coordinate the development of domestic semiconductor manufacturing technology. It has translated its mission into operating programs that are responsive to market forces and consistent with its identity as a consortium. It can point to an extensive inventory of important projects underway. It is reshaping relationships between U.S. chipmakers and their suppliers. And it has spurred new interest in cooperative research in industry, government, and academe. A withdrawal or significant reduction of federal support for the consortium could seriously jeopardize the consolidation and continuation of these accomplishments.

(2) Maintaining Current Federal Investment Levels

The Administration has included funding for SEMATECH at the current $100-million level in its FY 1991 Budget. The consortium has not sought an increase in this amount and it is not clear that additional funding could be quickly and productively absorbed. SEMATECH did not achieve its originally-projected $200-million/year spending rate until late in 1989. In addition, a proposal to raise the federal share of SEMATECH's budget could encounter resistance outside and inside the consortium. Though it has provided for continued funding of SEMATECH at current levels, the Administration has firmly rejected proposals to increase the federal contribution. Moreover, if the 50/50 joint funding formula continued to apply, increased federal funding for SEMATECH would require a commensurate increase in private funding, which could strain the consortium's smaller members.

Finally, a larger budget in the near term is probably not essential to the achievement of SEMATECH's principal technology development goals as articulated in 1989, or to the success of its current effort to reinforce key segments of the U.S. equipment industry, or to prospects for long-term cooperation between U.S. chipmakers and their U.S. suppliers.

(3) Increasing Federal Funding Substantially in the Short-Term

Increasing SEMATECH's budget by $100 million in the near term, as proposed by the NACS, could reduce risks inherent in the consortium's R&D enterprise. SEMATECH would be able to fill important "holes" and create "useful redundancies" in its project agenda.[1] It could also commit additional resources to the development of a full-flow demonstration environment and increased on-site testing of unsolicited equipment and materials. As noted above, however, these program enhancements are probably not essential to the achievement of the consortium's objectives as articulated in 1989.

(4) Increase Federal Funding by a Large Amount Over the Next Three Years

Increasing SEMATECH's budget by a large amount over the next three years would also entail shifting the consortium's R&D focus toward high-cost, long-term projects (e.g., projects to develop X-ray and excimer laser lithographic technology, advanced device concepts, and new materials). It is unlikely that all of SEMATECH's members share an interest in such projects, or that all of them would be ready to shoulder resulting increases in their membership fees. In addition, large long-term projects that appeal mainly to SEMATECH's largest members would conflict with the consortium's evolving corporate culture, which is inclusive, cooperative, and responsive to near-term market conditions.

Raising federal support for semiconductor R&D to the level suggested by the NACS would also represent a major extension of current policy. Such a change should be considered apart from the question of whether SEMATECH needs a larger budget to meet its own measured technology development goals. If the opportunity presented itself, SEMATECH could serve as the vehicle for a much expanded national semiconductor initiative. Given the range of federal R&D support authorities and programs related to semiconductors, however, SEMATECH would not be the only choice for such a task, or necessarily the best one.

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[1] The question of how SEMATECH would use additional funding was addressed by Bob Noyce (12/11/89) and Tom Seidel (12/14/89) in interviews for this report. "Holes" in the consortium's project agenda include assembly operations and packaging materials; examples of "useful redundancies" include increased investments in E-beam and step-and-scan lithographic technologies in addition to SEMATECH's current emphasis on optical steppers.